Figure 2.10. An example of logic networks.
Figure 2.14. The Venn diagram representation.
Figure 2.15. Verification of the distributive property

\[ x \cdot (y + z) = x \cdot y + x \cdot z \]
Figure 2.16. Verification of 

\[ x \cdot y + \bar{x} \cdot z + y \cdot z = x \cdot y + \bar{x} \cdot z. \]
Figure 2.32. Implementation of the function in Figure 2.31.
Figure 2.33. Implementation of a multiplexer.
Figure 2.35. A typical CAD system.
Figure 2.62. Two implementations of the function \( f(x_1, \ldots, x_4) = \Sigma m(2, 4, 5, 6, 10) + D(12, 13, 14, 15) \).
Figure 2.63. Using don’t-care minterms when displaying BCD numbers.
Figure 2.64. An example of multiple-output synthesis.
Figure 2.65. An example of multiple-output synthesis.
Figure 2.67. Karnaugh maps for Example 2.26.
Figure 2.68. Karnaugh maps for Example 2.27.

(a) Determination of the SOP expression

(b) Determination of the POS expression
Figure P2.5. Circuit for problem 2.78.
Figure P2.6. Circuit for problem 2.79.