Figure 5.5. Gated SR latch.
Figure 5.7. Gated D latch.
Figure 5.9. Master-slave D flip-flop.
Figure 5.10. Comparison of level-sensitive and edge-triggered D storage elements.
Figure 5.13. Positive-edge-triggered D flip-flop with Clear and Preset.
Figure 5.15. T flip-flop.
Figure 5.23. A four-bit counter with D flip-flops.
Figure 5.24. A counter with parallel-load capability.
Figure 5.28. Ring counter.
Figure 5.32. Implementation of the schematic in Figure 5.30 in a CPLD.
Figure 5.61. A reaction-timer circuit.
module BCDcount (Clock, Clear, E, BCD1, BCD0);
    input Clock, Clear, E;
    output reg [3:0] BCD1, BCD0;

    always @(posedge Clock)
    begin
        if (Clear)
            begin
                BCD1 <= 0;
                BCD0 <= 0;
            end
        else if (E)
            if (BCD0 == 4'b1001)
                begin
                    BCD0 <= 0;
                    if (BCD1 == 4'b1001)
                        BCD1 <= 0;
                    else
                        BCD1 <= BCD1 + 1;
                end
            else
                BCD0 <= BCD0 + 1;
        end
    endmodule

Figure 5.62. Code for the two-digit BCD counter in Figure 5.27.
Figure 5.67. A 4-bit counter.
Figure 5.73. Circuit for Example 5.20.
Figure 5.75. A faster 4-bit counter.