ECE/CS 3700
Digital System Design

Lecture Slides for Chapter 2: Universal Logic

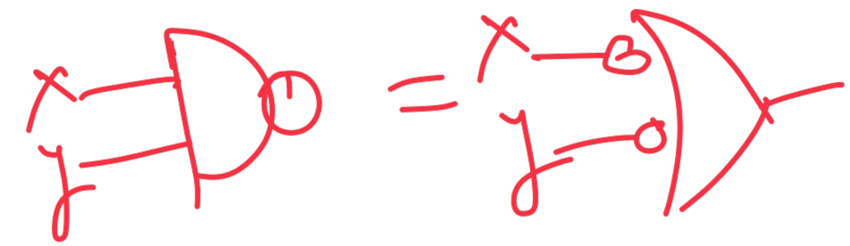
Priyank Kalla
Professor
Electrical & Computer Engineering

Universal Logic

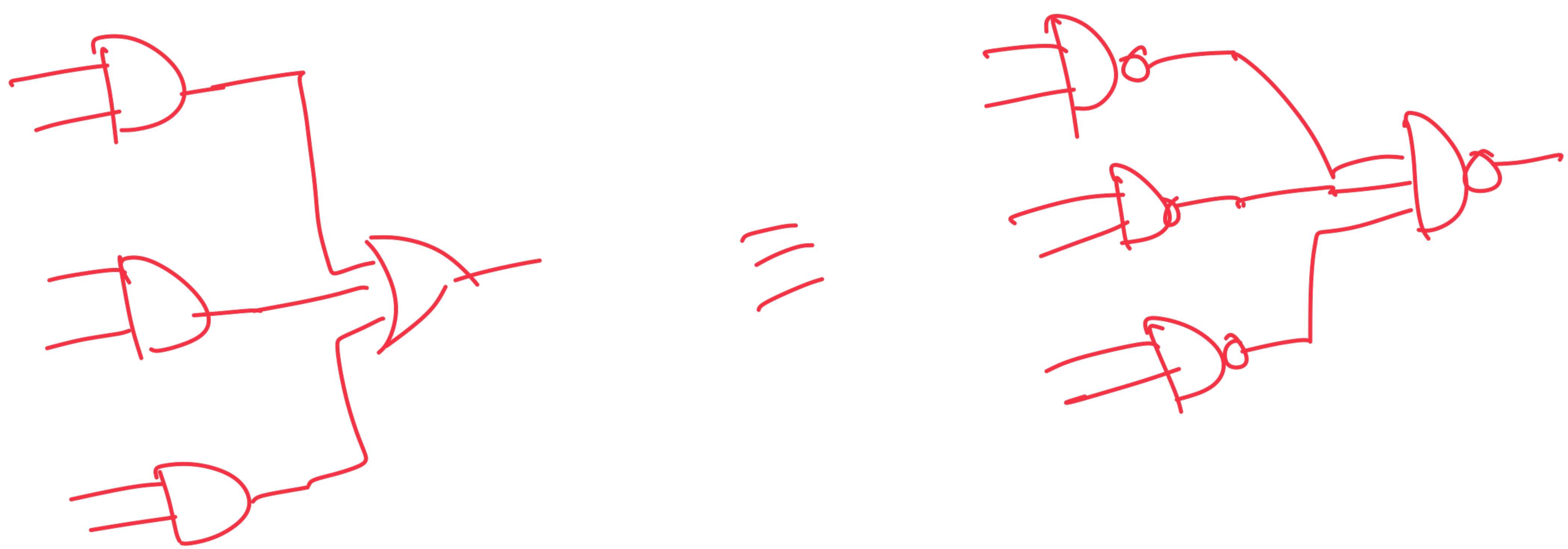
- A set of logical operators that can implement any arbitrary Boolean function
    - $\{AND, OR, NOT\}$: collectively implement any Boolean function: universal logic
    - ANDs and NOTs implement on-set minterms
    - OR of on-set minterms = function
    - Example: Majority function $f = a'bc + ab'c + abc' + abc$
- Only NAND gates = universal logic [important, PLAs]
- Only NOR gates = universal logic [important, PLAs]
- Only MUXes = universal logic [important FPGAs]
- $\{AND, XOR\}$ is also universal logic [important, to show off your mathematical reasoning prowess!]

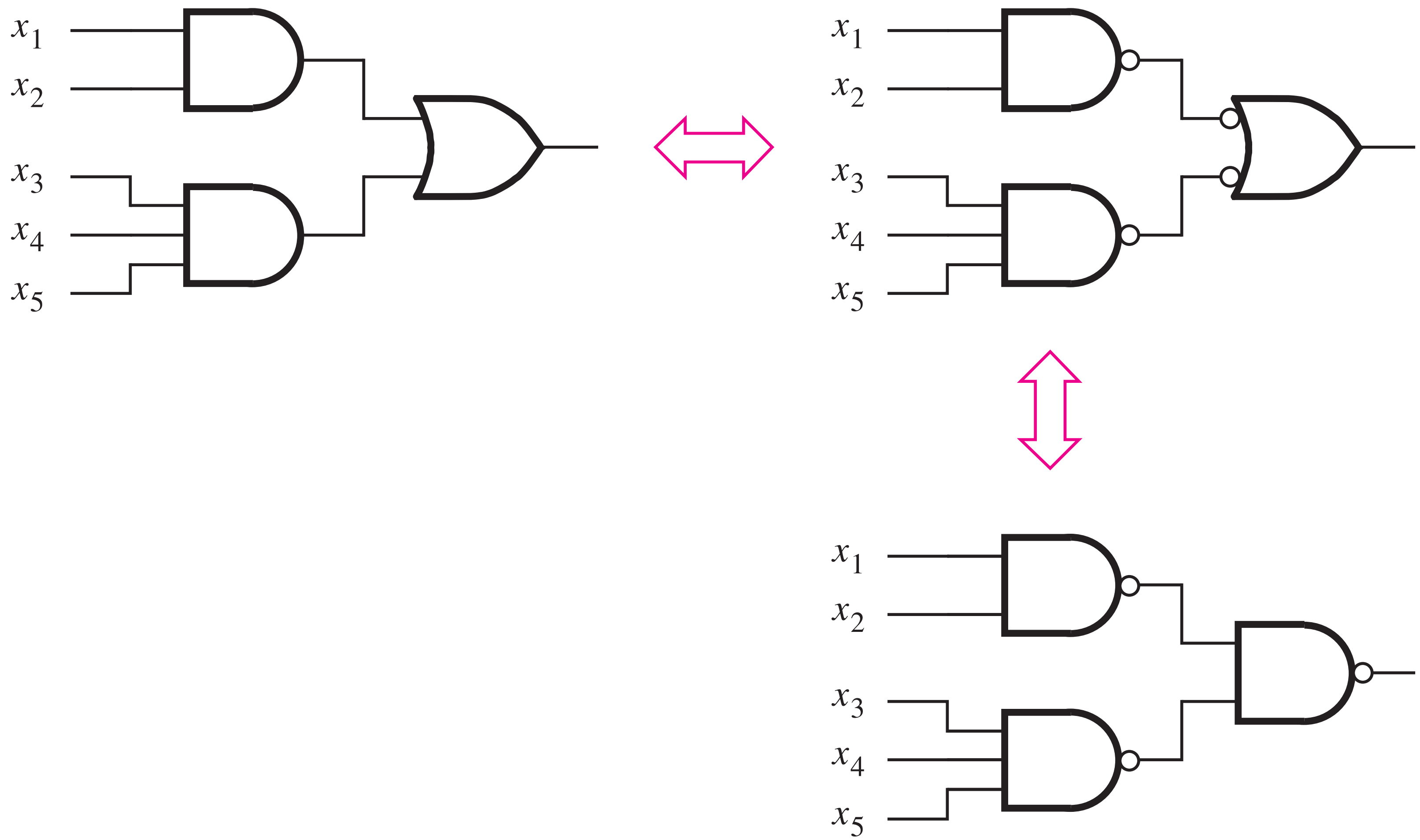
Boolean functions implemented with only NAND gates

- Relies on DeMorgan's laws: $\overline{x \cdot y} = \bar{x} + \bar{y}$



- $f = ab + ac + bc$



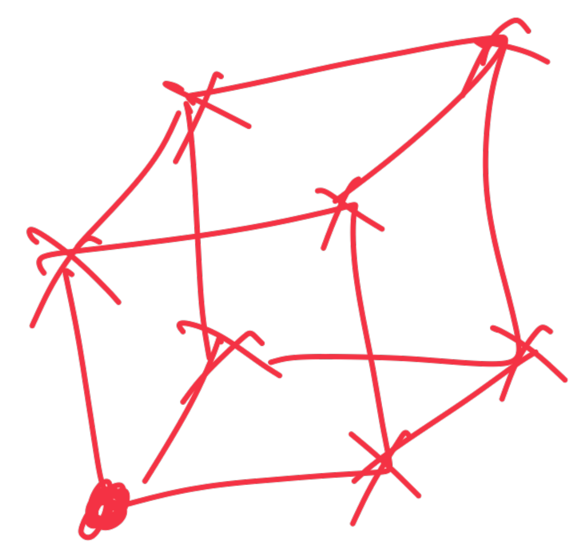

x_1
x_2
x_3
x_4
x_5
x_1
x_2
x_3
x_4
x_5
x_1
x_2
x_3
x_4
x_5

Maxterms and product of sum (POS) form

Row number	x_1	x_2	x_3	Minterm	Maxterm
0	0	0	0	$m_0 = \bar{x}_1\bar{x}_2\bar{x}_3$	$M_0 = x_1 + x_2 + x_3$
1	0	0	1	$m_1 = \bar{x}_1\bar{x}_2 x_3$	$M_1 = x_1 + x_2 + \bar{x}_3$
2	0	1	0	$m_2 = \bar{x}_1 x_2\bar{x}_3$	$M_2 = x_1 + \bar{x}_2 + x_3$
3	0	1	1	$m_3 = \bar{x}_1 x_2 x_3$	$M_3 = x_1 + \bar{x}_2 + \bar{x}_3$
4	1	0	0	$m_4 = x_1\bar{x}_2\bar{x}_3$	$M_4 = \bar{x}_1 + x_2 + x_3$
5	1	0	1	$m_5 = x_1\bar{x}_2 x_3$	$M_5 = \bar{x}_1 + x_2 + \bar{x}_3$
6	1	1	0	$m_6 = x_1 x_2\bar{x}_3$	$M_6 = \bar{x}_1 + \bar{x}_2 + x_3$
7	1	1	1	$m_7 = x_1 x_2 x_3$	$M_7 = \bar{x}_1 + \bar{x}_2 + \bar{x}_3$

Figure 2.22 Three-variable minterms and maxterms.

$M_0 = \overline{m_0}$



m_0

$M_0 = X$

Maxterms and POS forms

Row number	x_1	x_2	x_3	$f(x_1, x_2, x_3)$
0	0	0	0	0
1	0	0	1	1
2	0	1	0	0
3	0	1	1	0
4	1	0	0	1
5	1	0	1	1
6	1	1	0	1
7	1	1	1	0

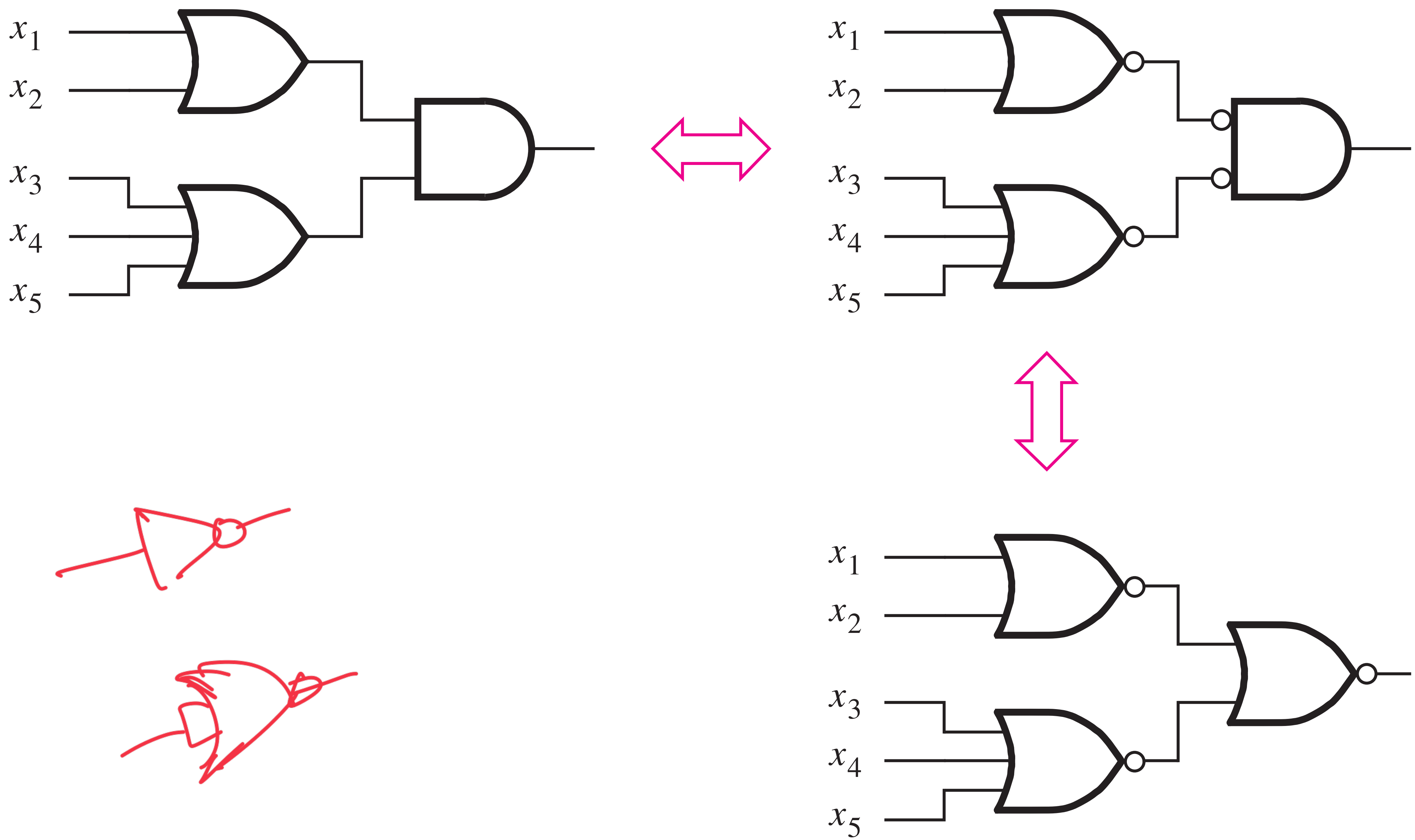
$$\overline{f}(x_1, x_2, x_3) = m_0 + m_2 + m_3 + m_7$$

Then f can be expressed as

$$\begin{aligned} f &= \overline{m_0 + m_2 + m_3 + m_7} \\ &= \overline{m}_0 \cdot \overline{m}_2 \cdot \overline{m}_3 \cdot \overline{m}_7 \\ &= M_0 \cdot M_2 \cdot M_3 \cdot M_7 \\ &= (x_1 + x_2 + x_3)(x_1 + \overline{x}_2 + x_3)(x_1 + \overline{x}_2 + \overline{x}_3)(\overline{x}_1 + \overline{x}_2 + \overline{x}_3) \end{aligned}$$

$$f(x_1, x_2, x_3) = \Pi(M_0, M_2, M_3, M_7)$$

$$f = \Sigma(m_1, m_4, m_5, m_6)$$



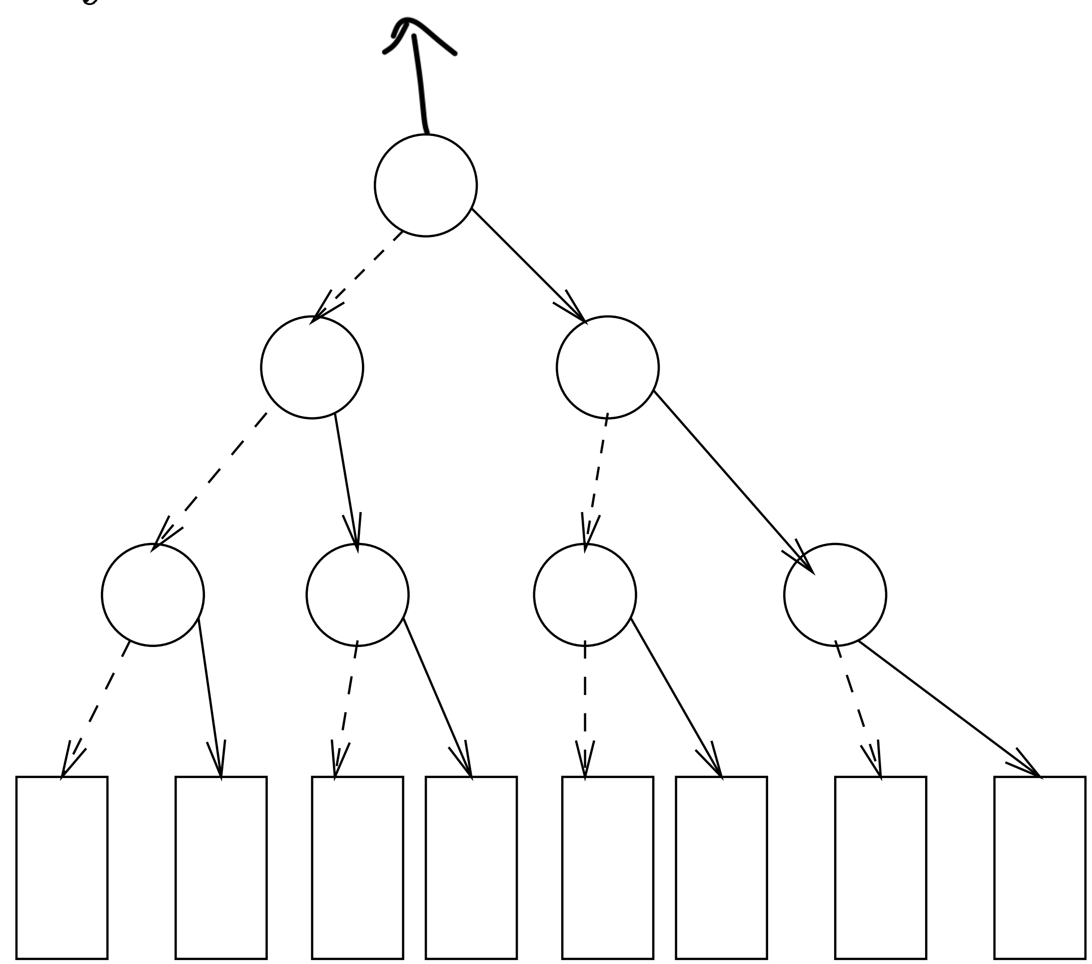
x_1
x_2
x_3
x_4
x_5
x_1
x_2
x_3
x_4
x_5
x_1
x_2
x_3
x_4
x_5

MUXes as Universal logic

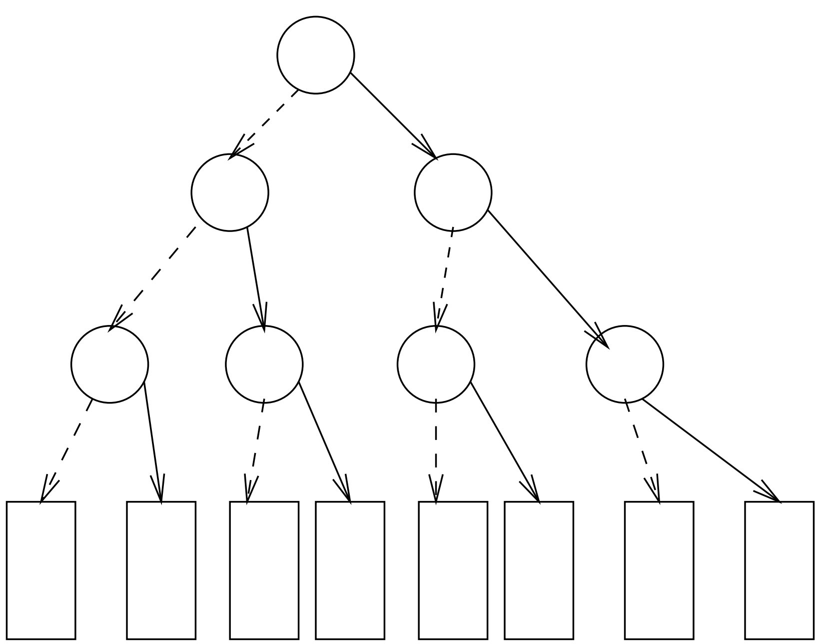
Truth Tables as Decision Trees (BDD)

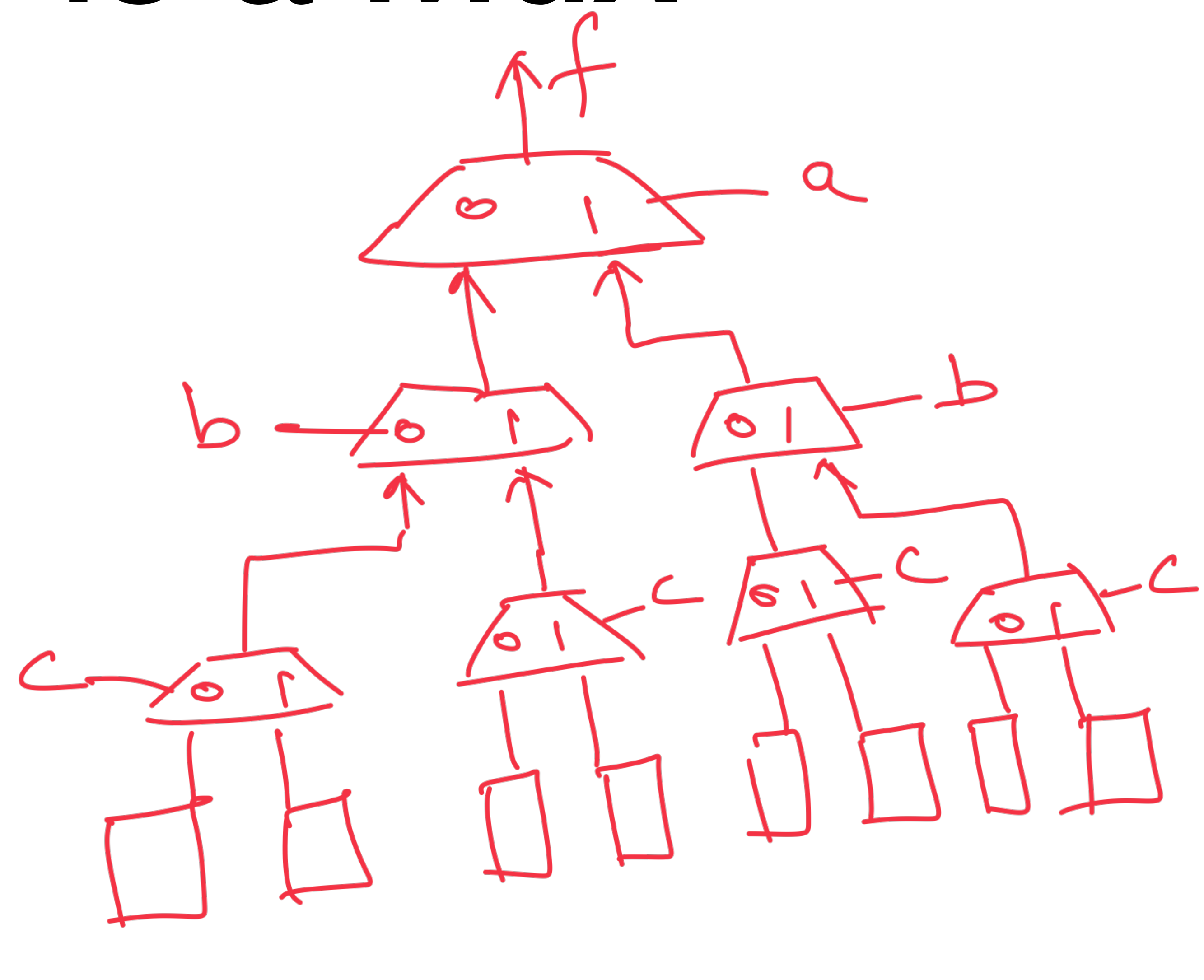
Truth Table versus Binary Decision Tree or Diagram

a	b	c	f
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1



Each node in the BDD (graph) is a Mux





From a truth-table to a BDD to only MUXes: universal logic!
This is what FPGAs are like….

AND-XOR is universal logic

- $f = a + b = a \oplus b \oplus (a \cdot b)$
- $f = \overline{a} = 1 \oplus a$

$x\bar{y} + \bar{x} \cdot y = x \cdot 1 + 0 = x$

$x \cdot 0 + \bar{x} \cdot 1 = \bar{x}$