Synchronizing sequences:

Fault-free machines to the same states. Concept of fault-free machines and fault-free machines.

In absence of resets, how to synchronize both fault and fault-free machines.

The concept of state distinguishing sequences.

How to distinguish between fault and fault-free machines?

How to distinguish between other words, traverse to other states.

The next state line, but not to Po? Unroll the machine, or in the next state line? Fault can be propagated to.

Bottlenecks: Fault activation requires an "activation state."

Procedure: Activate a fault, and propagate it to Po

(starting state available, sometimes not!)

Given: A sequential circuit, generate ATPG. Sometimes reset.

Sequential Circuit Testing: Problems
\[ I = \varepsilon x, 0 = \varepsilon x, I = I, x = 0 x : \bullet \]

...until...

Reset state: (00). Start in (00), and traverse the machine.

Reset Available
How? Using state distinguishing experiments.

You can distinguish between faulty and fault-free states of the machine.

Sometimes in the future, you can catch that effect.

Machine operation diverges...

Faulty and fault-free machines go to different states.

Fault DOWN gets into next state line.

Meaning of the above Test:
state. i.e., you can get a common starting point and fault-free machines can be initialized to a common initial state. 

- Called self-initializing tests. This test implies that both fault

- "control" the FPs (control the state).

  "control" backward in time from F.P. state (where you can

  you can get unknown values in FPs. This implies there exists a

  Answer: Sequential backtrack until the m/c backwards until

  Problem: How to get to the fault excitation state?

  

  \[ x = I \] propagates the fault effect.

  

  No reset state. Start w/ Fault excitation state: \( y_1 = 0, y_2 = 1 \).
Try to go back in previous time frames and try to get unknown values in P.P.s.

D and Y2 = I. Fault has an effect.

= 0 = x Y1 = 1. Fault excitation state: (11). Note: in this state, x

Take Ckt I. Assume no reset.

Self Initialization Test: NOT ALWAYS POSSIBLE
Lack of synchronization. But this does not imply redundancy.

Conclusion: Irredundant m/c can have unstable faults due to

one

The problem of synchronizing sequences - not every in/c has

"synchronized" to a common state.

Above implies that both faulty and fault-free m/c can be

back in time frames, until you can get unknown values in FPs

When NO RESET: start from fault excitation state and go

Faulty problem = distinguish faulty and fault-free states

Fault effect goes into FPs = faulty state transitions

Irredundant sequential w/ Reset = easy.

Seq. Circuit Testing concepts covered so far.
Sequential ATPC - the Pull Problem
Can you get to the F.E. state? Backward traversal.

(Forward traversal).

Given: No reset. Find P.E. Start. Propagate fault effect to Po.
Y2 = y_1'x + y_1y_2'
Y1 = y_1y_2 + y_1'y_2'x'

Untestable faults due to unreachable states
States (110) and (010) are equivalent, but cannot be distinguished.

What if fault takes me to 110 (faulty state), instead of 010 (fault free)?
Circuit of Redundant M/C