A Methodology for Thermal Characterization Abstraction of Integrated Opto-electronic Layouts

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***Abstract*—Hybrid integration of opto-electronic integrated circuits (OEICs) with CMOS electronics requires the modeling and characterization of thermal interactions. The thermal-gradient generated by the electronic layer causes modulation of the refractive index of the optical layers. This requires a thermal characterization for thermal-aware integration of OE-ICs. Full-scale, coupled, 3D electromagnetic and heat transfer simulation of the optical design is computationally infeasible. This paper describes a methodology and an abstraction model that, given external temperature hot-spots, computes a thermal gradient across the optical layout which can be used to estimate the deviation in operation of OEICs. The relative sparseness of optical layouts is exploited to employ a thermal resistance model. Our abstractions enable a compact 2.5D model for thermal computations, and techniques such as the Alternating Direction Implicit (ADI) method can be employed for numerical computations. The approach is applied on a fabricated silicon (Si) photonic optical logic chip.**

I. Introduction

Silicon (Si) photonics offer the potential for low-latency, low-power and high-bandwidth interconnect solutions for on-chip communications fabrics [1], in addition to optical signal processing and computing [2]–[4]. On-chip integration of opto-electronic integrated circuits (OEICs), however, poses the problem of *thermal-aware synthesis*. Si-photonic modulators such as ring resonators (RRs), Mach-Zehnder interferometers (MZIs), etc., lie at the core of photonic network systems. Such OEICs are extremely sensitive to temperature-induced changes in refractive index, due to silicon's large thermo-optic coefficient of $dn/dT = 1.86 \times 10^{-4}/^{\circ}K$. Consider the 3D chip-stacking scenario shown in Fig. 1, where an optical network-on-chip (ONoC) is integrated with a multi-processor system. High-frequency switching of electronics in processor cores will result in elevated temperature hot-spots on the VLSI chip. The resulting temperature gradient across the optical substrate will cause thermo-optic variations, i.e. thermal modulation of the refractive index of the material. This will cause OEICs, such as RRs, to fall out of resonance, causing the optical layer to function incorrectly.

To overcome this problem, various static and dynamic thermal-compensation schemes have been proposed [4]–[7]. These techniques compensate for *known temperature variations and their effects* by redesigning the ONoC [6] and their constituent RRs [7], by thermal-aware routing [5], or by way of operating system scheduling [4]. For such techniques to be successful, it is required to: i) compute the steady-state thermal gradient across the optical chip; and ii) couple the temperature information with optical/E&M analysis to estimate the deviation in OEIC functionality.

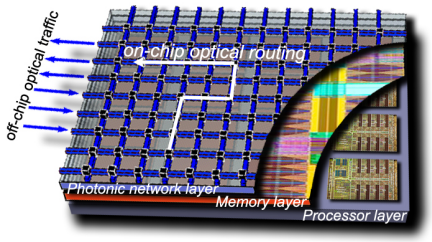


Figure 1: 3D stack: CMOS & OEICs. *Image Credit:IBM [8].*

This paper addresses the problem of computing the resulting thermal gradient of heat transfer to the optical substrate, together with the estimation of the deviation in device functionality in the thermally affected region. To compute a steady-state gradient for the 3D die-stacking topology of Fig. 1: i) the OEIC chip-layout is given; and ii) the externally-generated temperature hot-spots due to the electronic layer are given as a set of discrete heat sources Q_i placed at arbitrary locations (x_i, y_i) under the optical layer. We wish to compute the resulting gradient as it spreads through the photonic layer. We further relate optoelectronic device functionality with temperature in the thermally effected regions. Once determined, the impacted device's functionality can be compensated by relating temperature to a change in the refractive index (Δn) – which can be subsequently coupled to the phase of the signal for resonance analysis, etc.

Contributions: Performing full-scale, coupled, 3D electromagnetic and heat transfer simulations to achieve *thermal closure* for large designs is computationally infeasible. Therefore, the *paper presents an abstraction model and approach to compute the thermal gradient across the optical chip, and estimate OEIC performance, in an integrated fashion.* We exploit the fact that unlike VLSI, optical chip layouts are relatively sparse, and optical device sizes are an order of magnitude larger than CMOS gates; *e.g.* 90 - 150 nm waveguide thickness, 10 μm ring diameters are typical device sizes in contemporary optical device libraries. Therefore, the thermal effect modeling and characterization problems can be made scalable by exploiting this sparsity to derive an abstraction model. We utilize a *thermal resistance network* extracted specifically from the given optical layout. The gradient computation is then implemented using a finite

difference scheme, Alternating Direction Implicit (ADI) Method, which can utilize a Tridiagonal Matrix Solving Algorithm (Thomas Algorithm). Our approach effectively results in a compact 2.5D abstraction. The methodology was applied on an experimental optical logic chip, recently fabricated through the OPSIS foundry [9]. The paper describes this methodology and the abstraction model.

II. The Context of Previous Work

At the optical device-level, analysis of thermal effects on waveguides [10], [11] has been studied in terms of power, absorption, and phase. Athermal design of modulators is also proposed [12]. Our recent work [7] describes an automatic thermal-aware (re-)synthesis approach for the design of RRs. These topics have not been explored fully at the system level – particularly, w.r.t. their integration into design flow.

The work of [4] proposes an operating system level thermal-aware scheduling algorithm for managing traffic though an ONoC. On similar lines, [6] describes a ONoC recalibration and channel remapping methodology to compensate for thermally induced variations. Reduced-order steady-state thermal modeling and estimation techniques are not a subject of these works, but are assumed to be available.

Computation of thermal gradients on VLSI chips, with nanometer scale resolution, has been addressed by the EDA community [13]. Thermal-aware synthesis techniques make use of these algorithms for module placement [14] and routing [5], [15]. In contrast, we derive an *abstraction model and a methodology* to estimate the effect of an *external thermal gradient* on the operation of an optical layout.

III. Ring Resonators and Temperature Effects

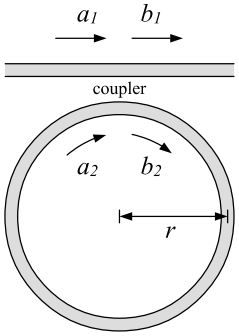


Figure 2: Structure of an Optical Ring Resonator

Optical RRs are wavelength filtering devices with a notch-filter-type response curve centered around a resonant wavelength. These devices rely on a resonance condition, which causes light within the ring to destructively interfere with light on the coupling waveguides. Alternatively, with two straight waveguides coupled to a single ring, a ring resonator can be used to couple specific wavelengths into or out of a waveguide in a 2x2-switch type operation. These RRs are used as switches and also to (de)multiplex multiple wavelengths on Si-waveguides in ONoCs.

Consider the RR structure depicted in Fig. 2, where a ring of radius r is coupled to a straight waveguide. The coupler is assumed to be symmetrical, and also lossless, implying that the coupling coefficient K is related to the transmission coefficient t by: $K^2+t^2=1$. The ring has an overall length of $L=2\pi r$, and round-trip loss coefficient α. The electric field amplitude E_{b_2} is the sum of the input electric field E_{a_1} coupled into the ring with coefficient K, and the round-trip feedback of the ring E_{a_2} coupled back into the ring with coefficient t. Likewise, E_{b_1} is the sum of the t-coupled input signal E_{a_1} and the K-coupled signal E_{a_2}. These are expressed as:

$$E_{b_2} = \frac{-jKE_{a_1}}{1-t\alpha e^{-j\phi}} \quad (1)$$

$$E_{a_2} = E_{b_2}\alpha e^{-j\phi} \quad (2)$$

$$E_{b_1} = tE_{a_1} - jKE_{a_2} \quad (3)$$

where $\phi=\beta L$ is the phase produced by the round-trip traversal of the ring from b_2 to a_2. Combining the above equations and squaring the result to determine power:

$$\frac{P_{b_1}}{P_{a_1}} = \left|\frac{E_{b_1}}{E_{a_1}}\right|^2 = \frac{\alpha^2+|t|^2-2\alpha|t|\cos\phi}{1+\alpha^2|t|^2-2\alpha|t|\cos\phi} \quad (4)$$

The value of Eqn. (4) drops to zero (0) when two conditions are met: critical coupling, and the resonance condition. At critical coupling, $\alpha=|t|$, and since ideally the ring is considered lossless, $\alpha=|t|=1$ and $K=0$. The *resonance condition* that constrains the round trip phase of the ring is defined as $\phi=\beta L=2\pi m$, where m is an integer. The dependence of ϕ on β implies that resonance is wavelength and waveguide (i.e. effective index) dependent and a useful relationship is derived:

$$\beta L=\frac{2\pi n_{eff}}{\lambda}L=2\pi m \quad \rightarrow \quad n_{eff}L=m\lambda \quad (5)$$

where n_{eff} is the effective index of the RR waveguide and λ is the resonant wavelength. Relating refractive index to temperature: $n=n_0-\frac{\partial n}{\partial T}\cdot(300K-T)$, where $\frac{\partial n}{\partial T}$ is the thermo-optic coefficient as a function of temperature, $(\frac{\partial n_{eff}}{\partial T})_{\mathrm{Si}}\approx 1.86\times10^{-4}$, and $0.62\times10^{-5}\leq(\frac{\partial n_{eff}}{\partial T})_{\mathrm{SiO_2}}\leq 1.28\times10^{-5}$. Therefore, temperature changes the refractive index directly, producing a transient effect on signal propagation:

$$\Delta\phi=\frac{2\pi}{\lambda}\Delta n_{eff}L=\frac{2\pi}{\lambda}L\frac{\partial n_{eff}}{\partial T}\Delta T \quad (6)$$

This change in phase causes changes to the interference pattern and the RRs fall out of resonance.

The Overall Methodology: Fig. 3 depicts the overall view of our problem and our approach. Given an optical layout and heat sources $Q_1, Q_2, Q_3, \ldots, Q_k$, we estimate the effect of these heat sources on the operation of the ring. The circumference of the ring waveguide is partitioned into

segments L_i, such that ring length $L = 2\pi r = \sum_i L_i$. For each of these segments L_i, the temperature T_i of that silicon waveguide segment is computed/estimated using the temperature-gradient computation. This temperature T_i can be coupled to effective index n_i of that waveguide segment using Eqn. (6), which is then averaged over the entire ring. For example, if $L = \sum L_i$, then the effective index is *estimated* as $n_{eff} = \frac{\sum_i n_i \cdot L_i}{L}$. Overall, we estimate the effect of heat sources on these individual grids, where the grid mostly contains materials such as the silicon guiding layer (waveguide), the oxide cladding, and the P+ and N+ doped regions to cause modulation. To compute this average temperature of a grid region, we employ a thermal resistive model and build a *layered abstraction*, which is described in the subsequent sections.

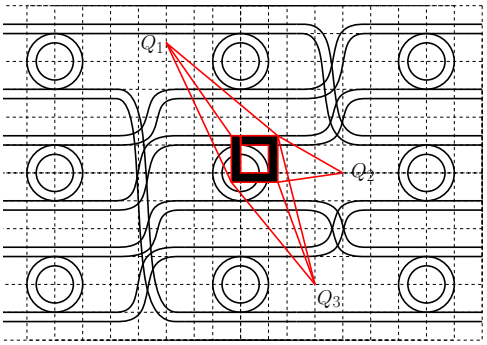


Figure 3: Layout with heat sources and emphasized block

IV. Physical Models and Numerical Formulation

Heat diffusion is governed by the following partial differential equation (PDE) [16]:

$$\rho C_p \frac{\partial T(\vec{r},t)}{\partial t} = \nabla \cdot (k(\vec{r},t)\nabla T(\vec{r},t)) + Q(\vec{r},t) \quad (7)$$

subject to the following boundary condition

$$k(\vec{r},t)\frac{\partial T(\vec{r},t)}{\partial n_i} + h_i T(\vec{r},t) = f_i(\vec{r},t) \quad (8)$$

where T is the temperature, $\vec{r}$ denotes the location, ρ is the material density, C_p is the specific heat, k is the thermal conductivity of the material, Q is the power density of the heat sources or sinks. Also, n_i, h_i, and f_i are normal to boundary surface i, the heat transfer coefficient and an arbitrary function at the surface i, respectively.

In formulating the model we can use a multi-grid resistance model for writing the heat transfer between nodes. Designating our node of interest, denoted with the subscript i, and the adjoining nodes, denoted with subscript j, we have the general-conduction-node situation, in which at steady state, the net heat input to node i must be must be zero or:

$$q_i + \sum_j \frac{T_j - T_i}{R_{ij}} = 0 \quad (9)$$

where q_i is the *heat flux* delivered to node i by heat generation, radiation, etc. The thermal resistance (R_{ij}) can take the form of convection boundaries, internal conduction, etc., and Eqn. (9) can be set equal to some residual for a relaxation solution or to zero for treatment with matrix and iterative methods.

In 3-dimensions, the 7-point finite-difference discretization of Eqn. (7) can be obtained through application of the backwards Euler formula results in an interior point formula,

$$\frac{T^{n+1}_{i,j,k} - T^{n}_{i,j,k}}{\Delta t} = \frac{T^{n+1}_{i+1,j,k} + T^{n+1}_{i-1,j,k}}{R_x} + \frac{T^{n+1}_{i,j+1,k} + T^{n+1}_{i,j-1,k}}{R_y} + \frac{T^{n+1}_{i,j,k+1} + T^{n+1}_{i,j,k-1}}{R_z} - 2 \cdot T^{n+1}_{i,j,k}\left(\frac{1}{R_x} + \frac{1}{R_y} + \frac{1}{R_z}\right) + Q_{grad} \quad (10)$$

where Δt, Δx, Δy, and Δz are discretized steps in temporal and spatial dimensions, respectively. R_x, R_y, and R_z are defined as

$$R_x = \frac{\Delta x}{k \Delta y \Delta z},\ R_y = \frac{\Delta y}{k \Delta x \Delta z},\ \text{and}\ R_z = \frac{\Delta z}{k \Delta x \Delta y} \quad (11)$$

For steady-state analysis, the term on the left in Eqn. (10) can be dropped, resulting in a linear algebra problem which can be solved numerically using Gauss-Seidel methods, successive over-relaxation (SOR), or the ADI Method. *As our earlier attempts at computing the thermal gradients on our experimental chip did not converge using the SOR method, we employ the ADI method.*

Alternating Direction Implicit (ADI) Method: The ADI method is a finite difference method for solving partial differential equations. The ADI method is an example of an *operator splitting* method which allow the unwieldy decomposition of PDE's into simpler subproblems and treats them individually (i.e. as *separable* problems). The form of the PDE to be studied is:

$$f = au_{xx} + au_{yy} + au_{zz} + su, \qquad (x,y,z) \in \Omega \quad (12)$$

where $\Omega \in \mathbb{R}^3$ is bounded on all sides. We also assume that mixed (Robin) boundary conditions are applied on all of $\partial\Omega$, and that a, s and f may all be functions of (x,y,z). Discretization of Eqn. (12) with backward difference approximations results in a system of linear algebraic equations that take the form: $Au = b$. Thus, A has the structure of a discrete Laplacian. In block notation the matrix has the following structure:

$$A = \begin{pmatrix} A_{xy} & -I & & & \\ -I & A_{xy} & -I & & \\ & -I & A_{xy} & -I & \\ & & -I & A_{xy} & \end{pmatrix} \quad (13)$$

$$A_{xy} = \begin{pmatrix} A_x & -I & & \\ -I & A_x & -I & \\ & -I & A_x & \end{pmatrix} \quad (14)$$

$$A_x = \begin{pmatrix} 6 & -1 & & & & \\ -1 & 6 & -1 & & & \\ & -1 & 6 & -1 & & \\ & & -1 & 6 & -1 & \\ & & & -1 & 6 & -1 \\ & & & & -1 & 6 \end{pmatrix} \quad (15)$$

Now we decompose the matrix A as $A = H + V + S$, where each of the matrices on the right-hand side is $n \times n$, and each comes from a specific term in Eqn. (12). The H, V, and S matrices arise in the discretization of the x, y, and z derivative terms, respectively.

The *tridiagonal structure* of these coefficient matrices allows for efficient tridiagonal algorithms that take advantage of the sparse structure. For example, the well-studied Tridiagonal Matrix Algorithm (Thomas Algorithm [17]) is a simplified Gaussian elimination specially formulated for the sparse structure of our coefficient matrix. For such a system, the solution can be obtained in $O(n)$ operations instead of $O(n^3)$ operations as required by a full Gaussian elimination. The ADI method is employed in our setting.

V. Model Abstraction

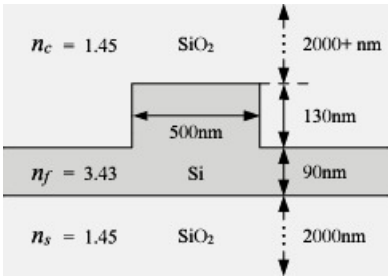


Figure 4: Waveguide Dimensions and Profile

Fig. 4 depicts the SOI ridge-waveguide profile and the dimensions that are used in our design. The types of materials and layout geometries we encounter in this investigation are mainly silicon (Si), doped regions, and silicon dioxide (SiO_2). The heat we expect to be delivered to certain boundary nodes is around $80 - 100\ W/cm^2$. The thermal resistance (R_{ijk}) can take the form of convection boundaries, internal conduction, etc. To express the overall effect of convection, we use Newton's law of cooling: $q = hA(T_{edge} - T_\infty)$. Here the heat-transfer rate is related to the overall temperature difference between the domain edge and the medium and the surface area A. The quantity h is called the *convection heat-transfer coefficient*. Typical values to expect are $h = 50 - 150\ W/(m^2K)$ for an optimized heat sink typically found in a desktop computer.

The heat transfer resistances are networked over the entire spatial domain as seen in Fig. 5. This is a linear approximation and we are only interested in the temperature at the nodes. These nodes correspond to each grid point in Fig. 3, corresponding to a segment of a waveguide.

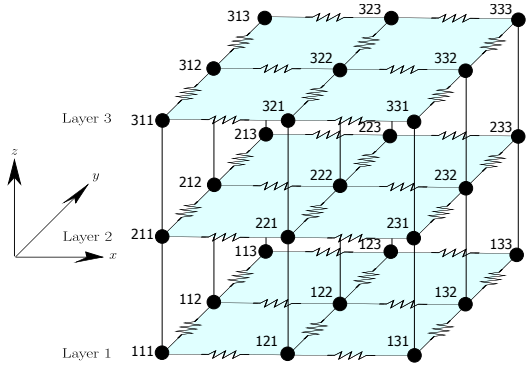


Figure 5: 3D Thermal Resistance Example

Each node has *six neighbors*, a *positive* and a *negative* step for each dimension. The explicit representation for the nodal formulation is

$$T_{xyz} = \frac{\sum_{(i,j,k)\in\mathbf{S}} \left(q_{ijk} + \frac{T_{ijk}}{R_{xyz\to ijk}} \right)}{\sum_{(i,j,k)\in\mathbf{S}} \left(\frac{1}{R_{xyz\to ijk}} \right)} \quad (16)$$

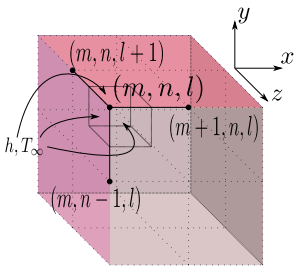
$$\mathbf{S} \in \{(x \pm 1, y, z), (x, y \pm 1, z), (x, y, z \pm 1)\} \quad (17)$$

where q_{ijk} is the *heat flux* delivered to node ijk by heat generation, radiation, etc. There are resistance modifications required to account for convection boundary conditions. An example of these nodal resistances, and the modifications necessary for the convection boundary nodes, is illustrated in Table I for a Corner Convection Node. Other boundary conditions can be similarly modeled.

The entire chip, in 3-dimensions, can of course be transformed into a uniform resistive grid as in Fig. 5, and the entire system of Eqns. (16)-(17) can be attempted to be solved by the ADI method. However, this will be prohibitive. We now show how this model can be abstracted *layer-by-layer*, exploiting the sparsity of optical layouts.

A. Abstraction of an Optical Layout

Given a photonic layout in GDSII format, and an external thermal gradient with dimensions relative to the layout, we partition our system into a resistive network. We construct this matrix based on the thermal conductivity composition of each square block (Fig. 5). Since we wish to estimate the effect of the gradient the on *individual devices* within the layout, we ensure a grid-resolution less than that of the



(a) Corner Convection

Condition	
$\mathbf{R_{m_+}}$	$\frac{4\Delta x}{k\Delta y\Delta z}$
$\mathbf{R_{m_-}}$	$\frac{4}{h_{m\_}\Delta y\Delta z}$
$\mathbf{R_{n_+}}$	$\frac{4}{h_{n_+}\Delta x\Delta z}$
$\mathbf{R_{n_-}}$	$\frac{4\Delta y}{k\Delta x\Delta z}$
$\mathbf{R_{l_+}}$	$\frac{4\Delta z}{k\Delta x\Delta y}$
$\mathbf{R_{l_-}}$	$\frac{4}{h_{l\_}\Delta x\Delta y}$

Table I: 3D Resistive Boundary Condition for Corner Convection

size of the devices. For the rest of the layout, we maintain a resolution of the width of a waveguide, $\sim 500\ nm$.

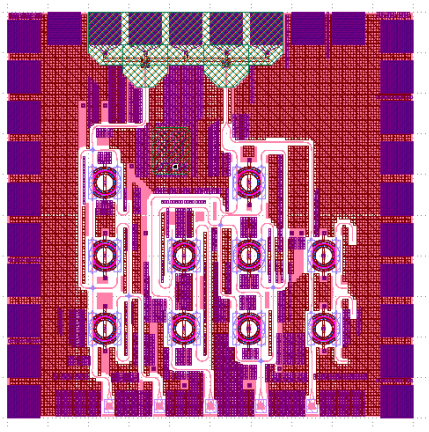


Figure 6: Optical Logic Design Layout

As evident from Fig. 4, the thickness of SOI cladding is much larger than the height of the Si guiding layer. This suggests a natural way to discretize the layout non-uniformly based on the thickness of the layered materials. The matrix is generated on a layer-by-layer basis as depicted in Fig. 7. We choose the layers such that they most accurately represent the changing dimensions in the z-direction. We import the layers one-by-one to generate a *two-dimensional representation in matrix form for each layer and connect them together by resistors – node ij of one layer connects to the corresponding node (ij) on the next layer.*

By analyzing the layout, we determine the ratio of

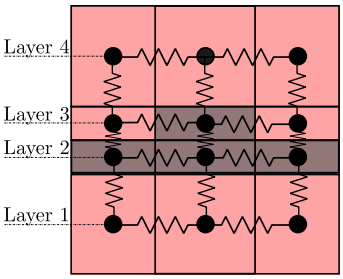


Figure 7: Networking Over the Third Spatial Dimension

materials (e.g., Si to SiO_2) in any square element area of our discretization and estimate the materials thermal conductivity by weighting the sums based on this ratio. For example, if we have $\sim 30\%$ of Si and $\sim 70\%$ of SiO_2 in the square element of interest, we can compose k_{eq} as $k_{eq} = 0.3 \cdot k_{Si} + 0.7 \cdot k_{SiO_2}$ where the k's are the thermal conductivities.

Fig. 6 depicts the GDSII layout of our optical logic chip designed using Si-RRs, waveguides, splitters, couplers, Bragg-gratings and Ge-detectors. The chip implements a Boolean adder using Si-RR based optical logic synthesis [3], whose placement and routing was performed according to [18]. The approach is applied to compute the steady-state thermal gradient on this chip, with a heat source placed (simulated) under the chip. The tool K-LAYOUT was modified and used to import the layout information, and the computation was implemented as an algorithm in MATLAB. The result of one such layered-3D simulation experiment for the layout is shown in Fig. 8. We see that silicon is taking the bulk of the heat flux due to its higher thermal conductivity. Heat does penetrate through the layers of the layout and stress individual devices. Using this information, deviation in device functionality can be estimated.

VI. CONCLUSIONS

The paper has described a methodology and a model for thermal characterization of integrated optical layouts. As optical devices are integrated with CMOS electronics, heat generated by switching of electronic circuitry acts as externally generated temperature gradient across the optical substrate. This change in temperature modulates the refractive index of the optical devices and causes their incorrect operation. Remedial measures require that such a deviation be estimated. We present a methodology that: i) provides a layer-by-layer abstraction of the layout into a 2.5D thermal resistance model, which is non-uniform and simplified in one dimension; ii) enables the use of efficient ADI methods for the resulting numerical computation of thermal gradients; and iii) shows how the change in temperature can be coupled to estimate the change of phase/interference of Si-photonic RRs. Result of a simulation experiment on a real chip was also depicted. Work is underway to compare the simulation results against measurements in the lab.

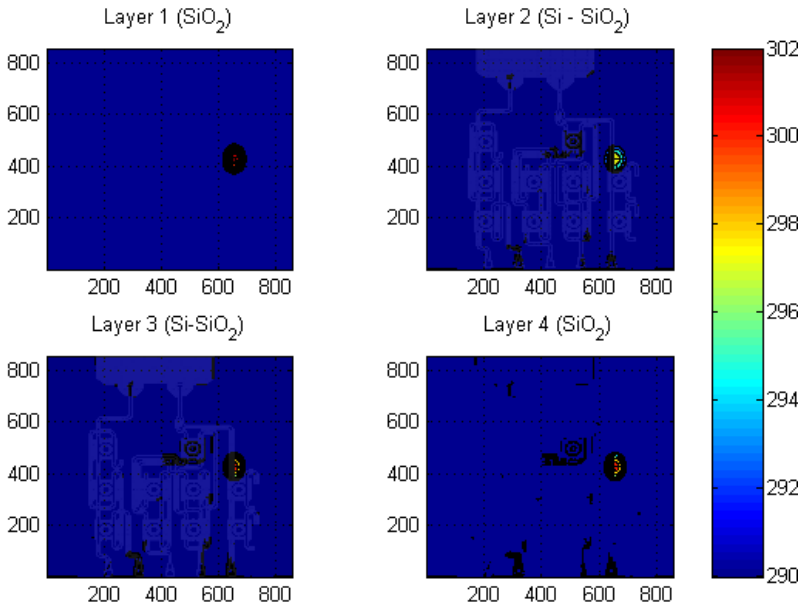


Figure 8: 3D-FDM Heat Conductance on Optical Layout

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