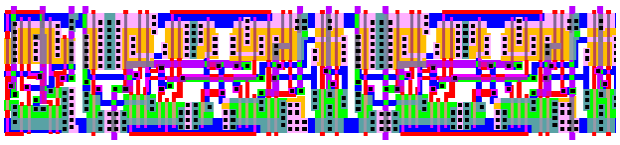
CS/EE 5710/6710
Digital VLSI Design



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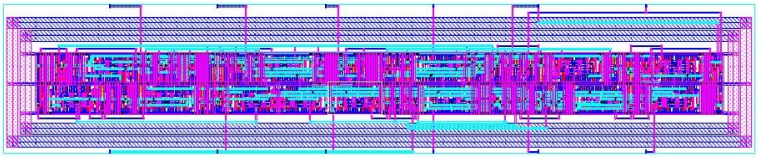


CS/EE 5710/6710

- Digital VLSI Design
  - T Th 5:15 - 6:35, WEB 2230
- Instructor: Prof. Ken Stevens
  - MEB 4506
  - Office hours: by appointment
- TA: Tannu Sharma and Venkata Bommu
  - Office hours: In the CADE lab
  - Primarily Monday and Tuesday??? Tell us!

CS/EE 5710/6710

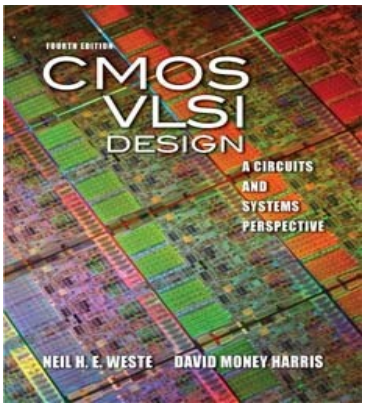
- Web Page - all sorts of information!
- www.eng.utah.edu/~kstevens/5710
- Contact:
  - 5710@list.eng.utah.edu
    - Goes to everyone in the class
    - We'll populate automatically, but to add an e-mail: http://sympa.eng.utah.edu/sympa
  - teach-5710@list.eng.utah.edu
    - Goes to instructor and TAs

Textbook

- Principles of CMOS VLSI Design

  Weste and Harris

  (4th edition)

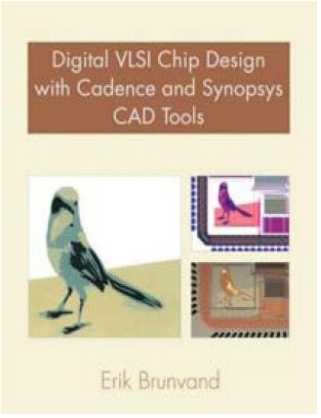


CAD Manual

- Written by Utah Prof. Brunvand
  - Describes in detail how to use the CAD tools
  - Tutorial in nature

  Based on v5 of the Cadence tools

  Revisions for v6 on the web.



Class Goal

- To learn about modern digital CMOS IC design
  - Class project – teams will build moderate sized chip
    - We'll form teams in a few weeks
  - These chips can be fabricated through MOSIS
    - Chip fabrication service for small-volume projects
    - Educational program funded entirely by MOSIS

Class CAD Tools

- We'll use tools from Cadence and Synopsys
  - These only run on Linux in the CADE lab, so you'll need a CADE account
    - I also assume you know something about UNIX
    - Lots of web tutorials exist if you need them...

Prerequisites

- Digital design is required! (i.e. CS/EE 3700)
  - Boolean algebra
  - Combinational circuit design and optimization
    - K-map minimization, SOP, POS, DeMorgan, bubble-pushing, etc.
    - Arithmetic circuits, 2's complement numbers
  - Sequential Circuit design and optimization
    - Latch/flip-flop design
    - Finite state machine design/implementation
    - Communicating FSMs
    - Using FSMs to control datapaths

Assignment #1 – Review

- On the class web site is a review assignment
  - If you can do these problems, you probably have the right background
  - If you can't, you may struggle!!!!!
- Please take this seriously! Give this homework consideration and make sure you remember what you need to know!
  - You also need to turn it in next week by Tuesday Sept 2nd
  - Must do independently, will be graded

Recommendations

- Computer Architecture experience is helpful
  - Instruction set architecture (ISA)
  - Assembly language execution model
  - Instruction encoding
  - Simple pipelining
- I assume you've used some sort of CAD tools for digital circuits
  - Schematic capture
  - Simulation

First Assignment

- CAD Assignment #1
  - Cadence Composer tutorial
  - Simple circuit design with simulation
    - Learn basic Verilog for testbench
  - Available on the web site
  - Due Thursday, September 9th, 5:00pm
    - E-mail submission with tar

» **START NOW!!!**

Assignments/Grading

- Labs (cell designs) & Homework (40%)
- Design review (5%)
- Mid-term exam (15%)
- Final Project (40%)
  - See the syllabus (web page) for more details about grading breakdown

Transistor Explosion

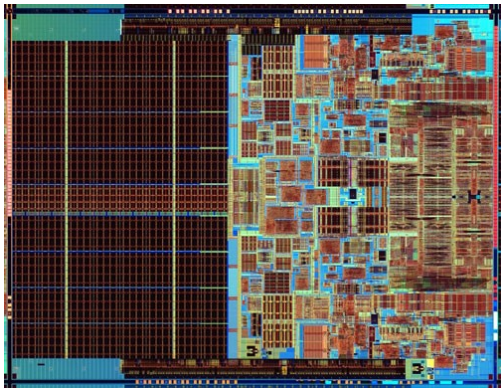
- 1958: First integrated circuit
  - Flip-flop using two transistors
  - Built by Jack Kilby at Texas Instruments
- By 2008:
  - Intel Core2 Duo – 291,000,000 transistors
- 53% compound annual growth rate over 50 years
  - No other technology has grown so fast so long
- Driven by miniaturization of transistors
  - Smaller is cheaper, faster, lower power
  - Revolutionary effects on society

Where are the Transistors?

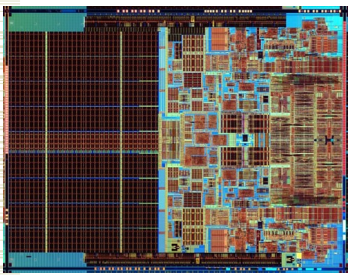
- 300 million transistors is a lot of logic!
- Where are they used?
  - Memory is single largest consumer.
  - SRAM has 6 transistors per bit
  - Intel Core2 Duo: 4MB shared L2 Cache, with 32K I-Cache, 32K D-Cache on each core
  - 4*1048576*8 + 2(64*1024*8) = 32,603,008
  - 32,000,000 bits * 6 = 207,618,048 trans.
  - Quad core design has around 820M transistors

Intel Core2 Duo

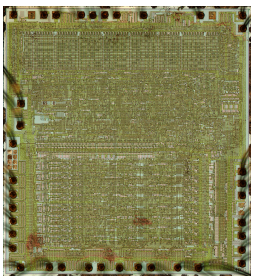
- 65nm process, 75W, 144mm^2 die



Historical Comparison



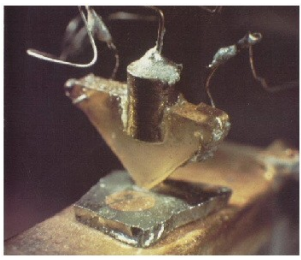
Core2 Duo
65nm devices
144mm2 die
291,000,000 transistors
over 4MB (32Mbit) of on-chip storage
2200MHz



6502 (Apple II, Nintendo NES etc.)
6000nm devices (6 micron (6000nm))
22mm2 die
3510 transistors (nmos only)
56 total bits of state
1MHz

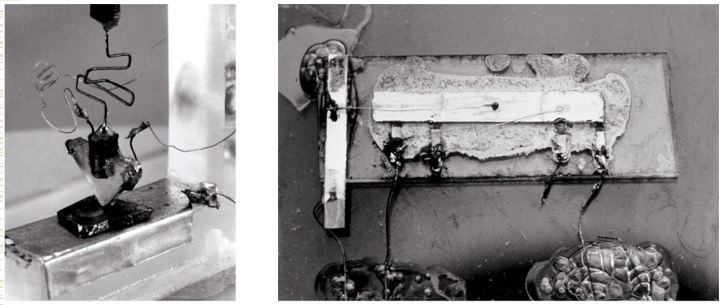
Transistor Revolution

- Vacuum tubes ruled the first half of 20th century: large, expensive, power-hungry, unreliable
- 1947: first point contact transistor
- Where are they used?
  - John Bardeen and Walter Brattain at Bell Labs
  - Read *Crystal Fire* by Riordan, Hoddeson



From Weste/Harris

First Integrated Circuit



(a) (b)

FIG 1.2 (a) First transistor (Courtesy of Texas Instruments.) and (b) first integrated circuit. (Property of AT&T Archives. Reprinted with permission of AT&T.)

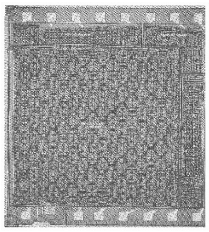
From Weste/Harris

Transistor Types

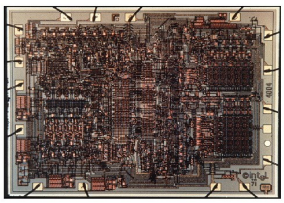
- Bipolar transistors
  - npn or pnp silicon structure
  - Small current into very thin base layer controls large currents between emitter and collector
  - Base currents limit integration density
- Metal Oxide Semiconductor FET (Field Effect Transistors)
  - nMOS and pMOS Metal Oxide FET Semiconductors (MOSFETS)
  - Voltage applied to insulated gate controls current between source and drain
  - Low power allows very high integration

MOS Integrated Circuits

- 1970's processes usually only had nMOS transistors
  - Power again an issue due to idle current



Intel 1101 256-bit SRAM



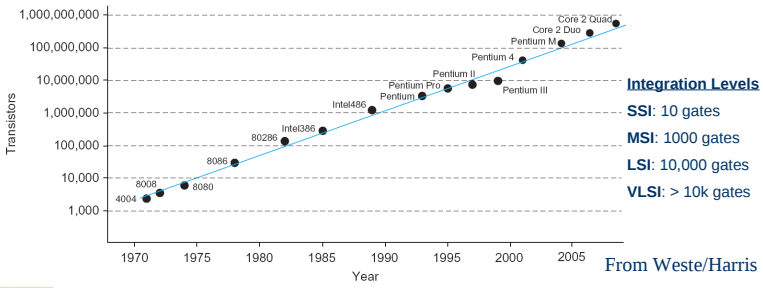
Intel 4004 4-bit µProc

From Weste/Harris

- 1980's to present
  - CMOS processes only have leakage

Moore's Law

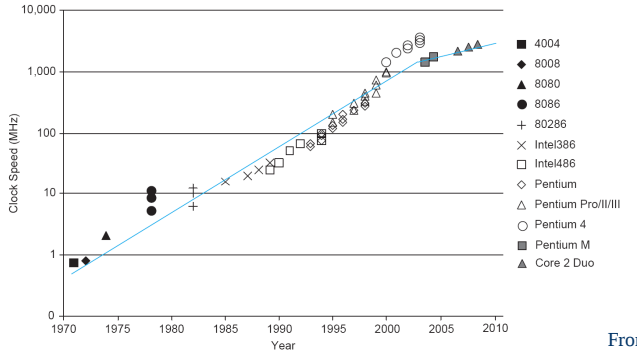
- 1965: Gordon Moore plotted transistors per chip
  - Fit straight line on semilog scale
  - Transistor counts have doubled every 26 months



From Weste/Harris

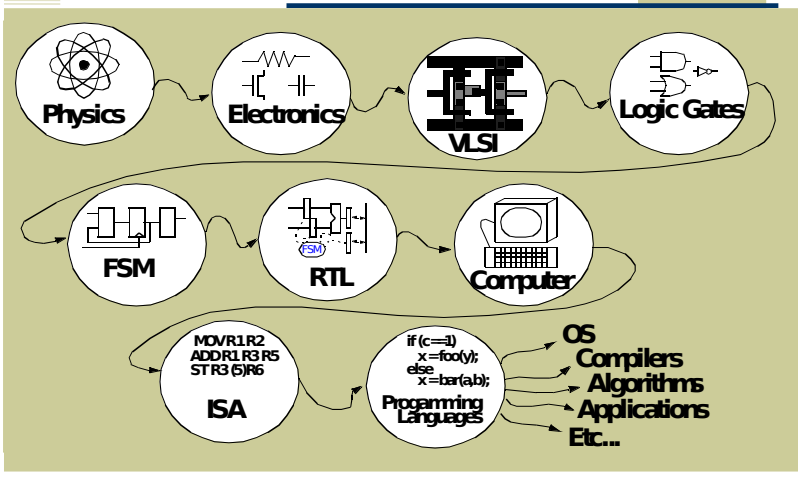
Corollaries

- Many other factors grow exponentially
  - E.g. clock frequency, processor performance

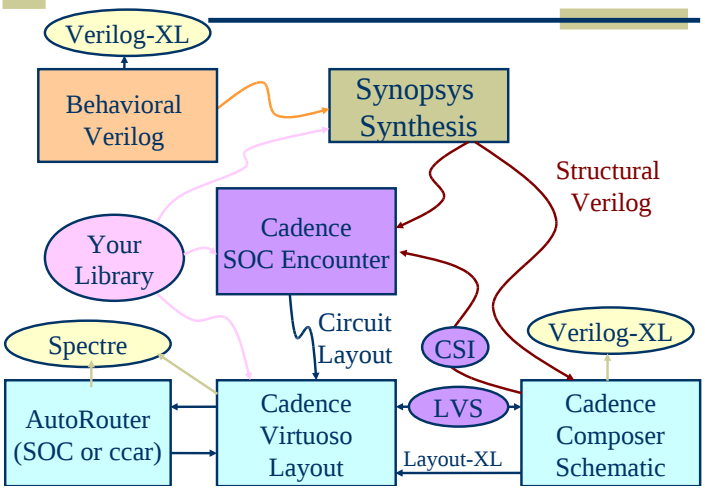


From Weste/Harris

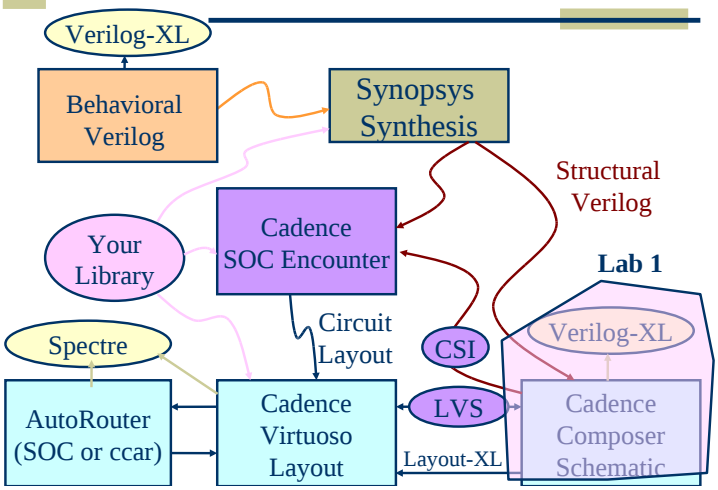
The Big Picture



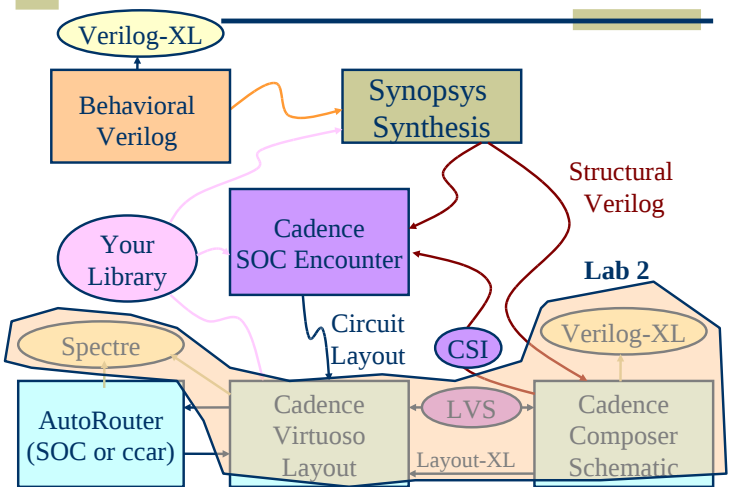
A View of the Tools



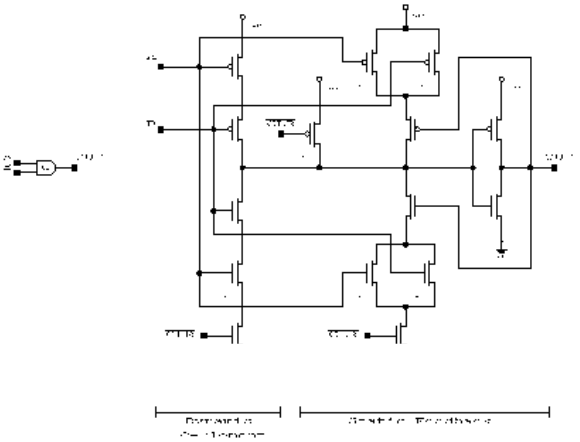
A View of the Tools



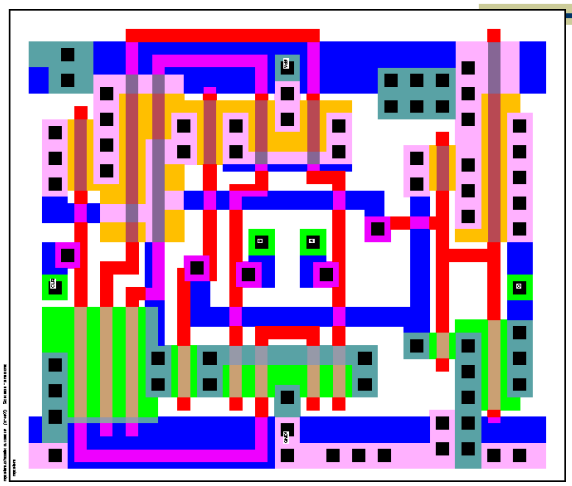
A View of the Tools



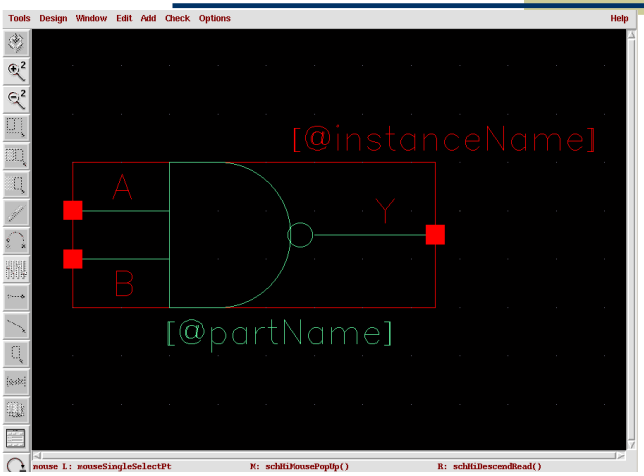
Circuits made from Transistors



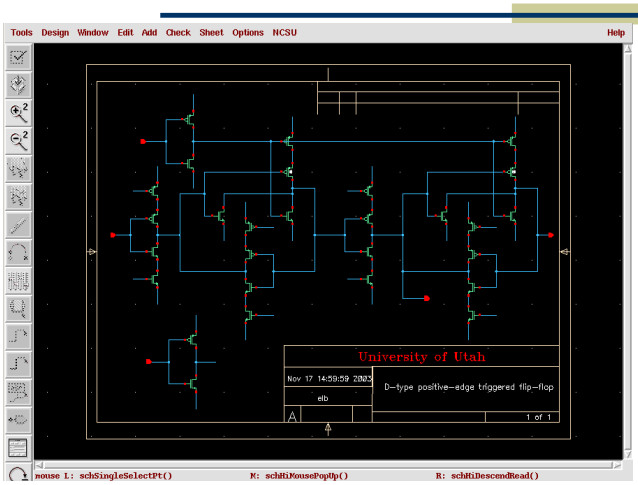
Convert Transistors to Layout



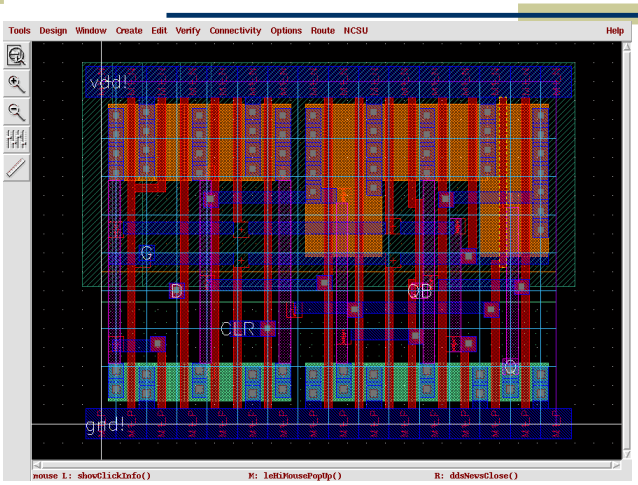
Cadence Composer Symbol



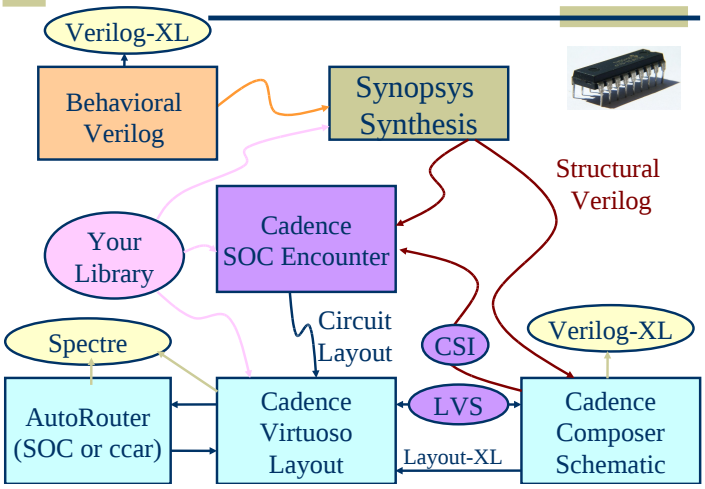
Cadence Composer Schematic



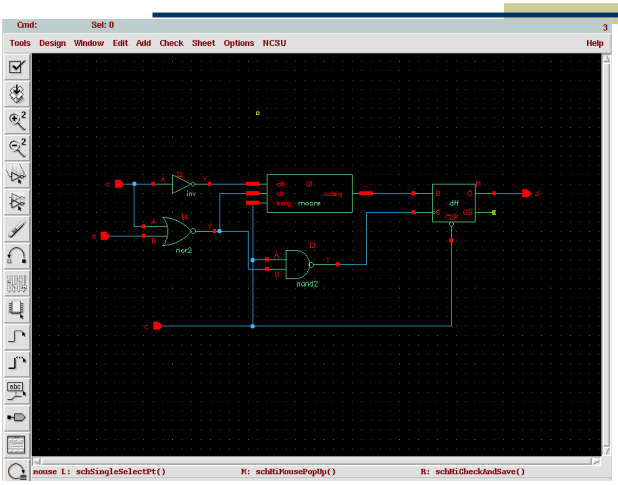
Cadence Virtuoso Layout



Chip Design with your Cells



Cadence Composer Schematic



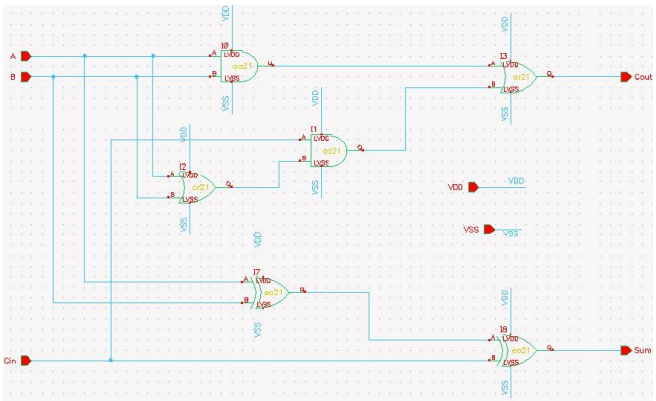
HDL Description

```
module moore (clk, clr, insig, outsig);
input clk, clr, insig;
output outsig;
// define state encodings as parameters
parameter [1:0] s0 = 2'b00,
s1 = 2'b01,s2 = 2'b10, s3 = 2'b11;
// define reg vars for state register
// and next_state logic
reg [1:0] state, next_state;
//define state register (with
//synchronous active-high clear)
always @(posedge clk)
begin
      if (clr) state = s0;
      else state = next_state;
end
```

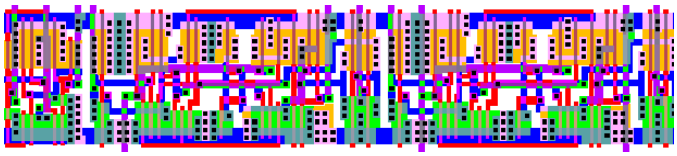
```
// define combinational logic for
// next_state
always @(insig or state)
begin
     case (state)
        s0: if (insig) next_state = s1;
            else next_state = s0;
        s1: if (insig) next_state = s2;
            else next_state = s1;
        s2: if (insig) next_state = s3;
            else next_state = s2;
        s3: if (insig) next_state = s1;
            else next_state = s0;
      endcase
end
// assign outsig as continuous assign
assign outsig =
((state == s1) || (state == s3));
endmodule
```

VLSI Design

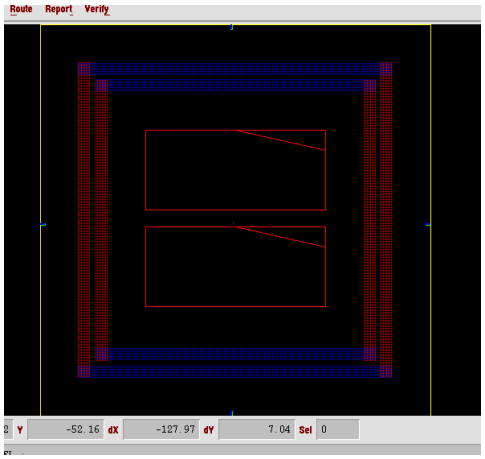
- Or start with a schematic (or a mix of both)



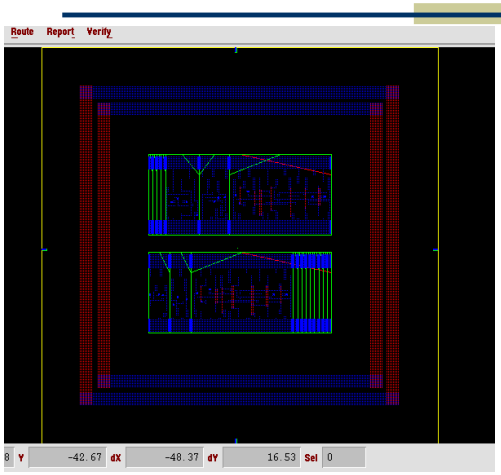
Assemble Gates into a Circuit



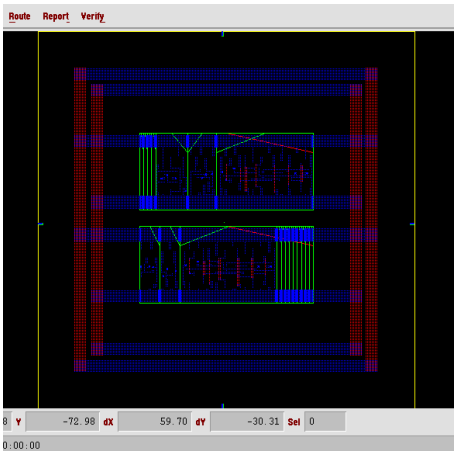
Standard Cells…Power Rings



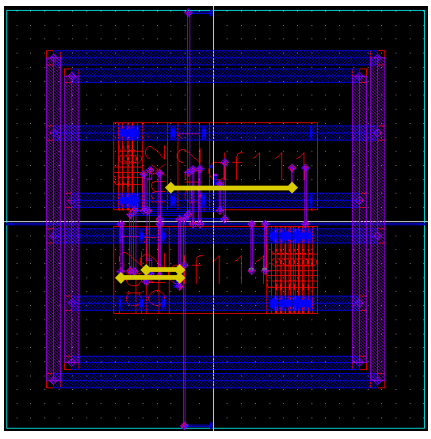
Place Cells and Fillers



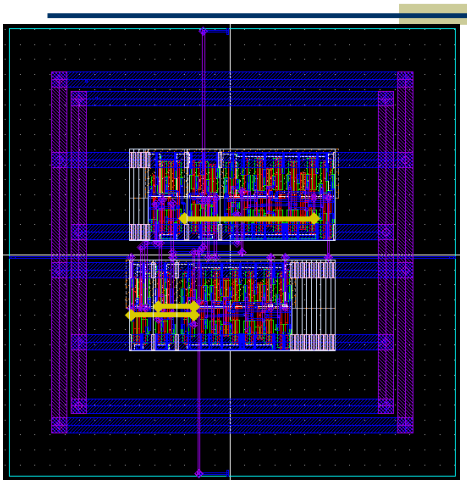
Connect Rows to Power



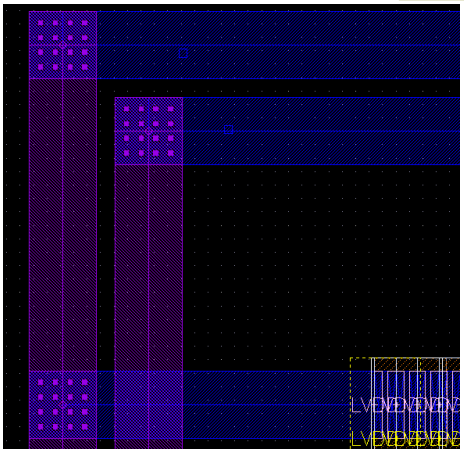
autoRouted View



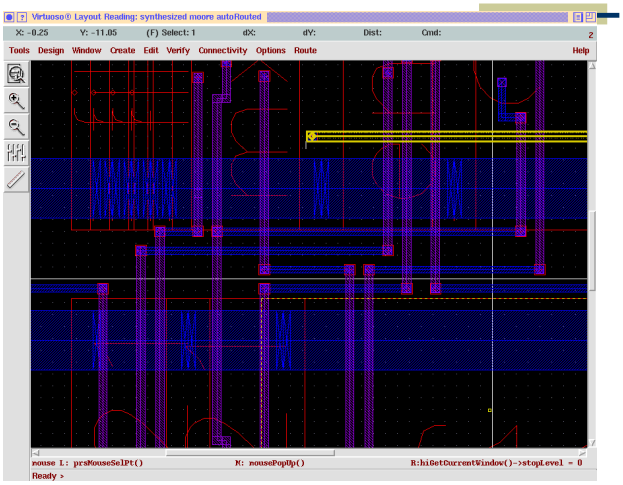
autoRouted Layout View



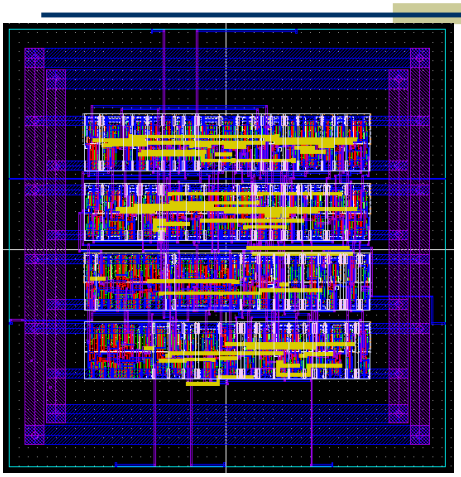
Corners…



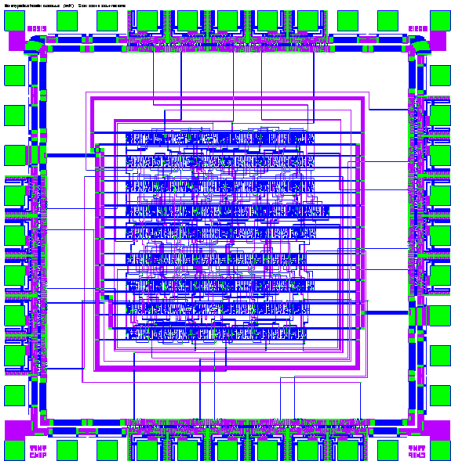
Routing



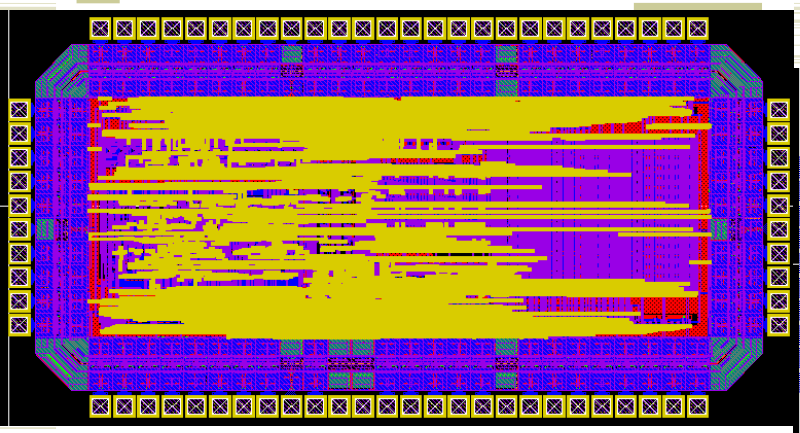
Slightly Larger Example



And Assemble Whole Chip



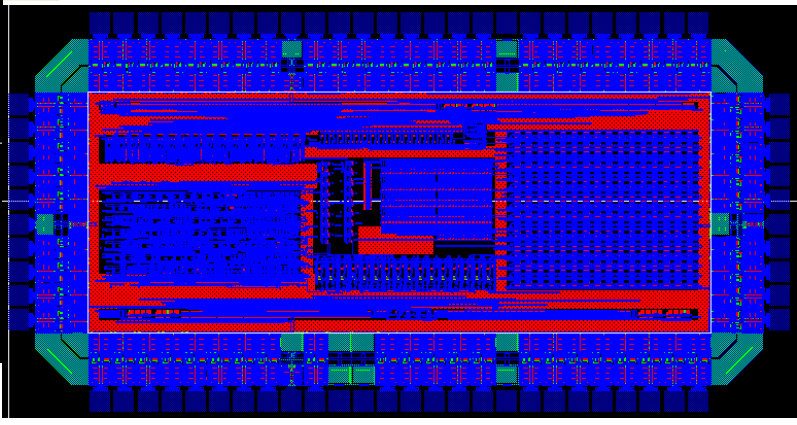
Example Class Chip (2001)



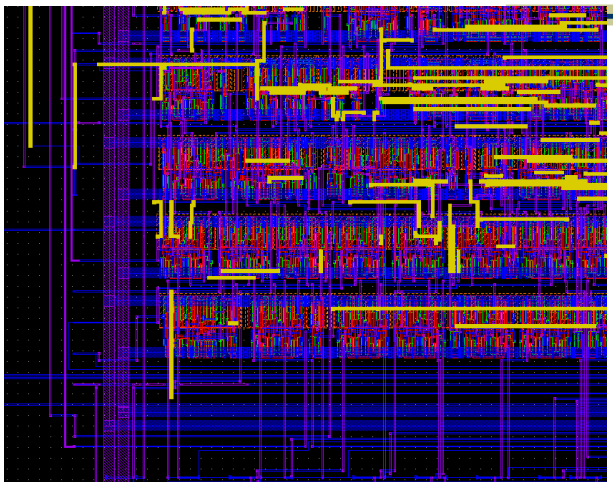
16-bit Processor, approx 27,000 transistors

Same Chip (no M2, M3)

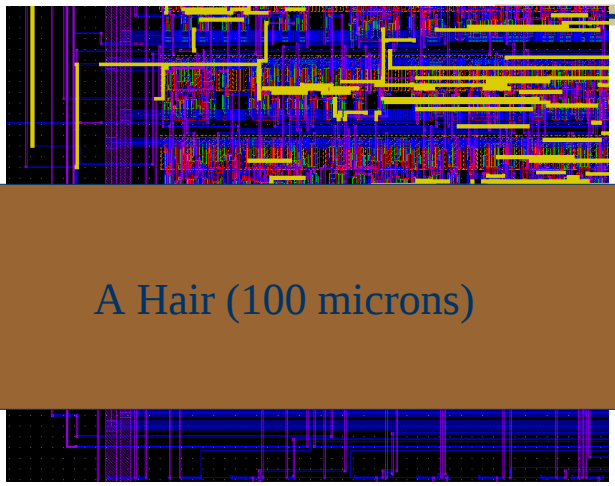
1.5mm x 3.0mm, 72 I/O pads



Zoom In…

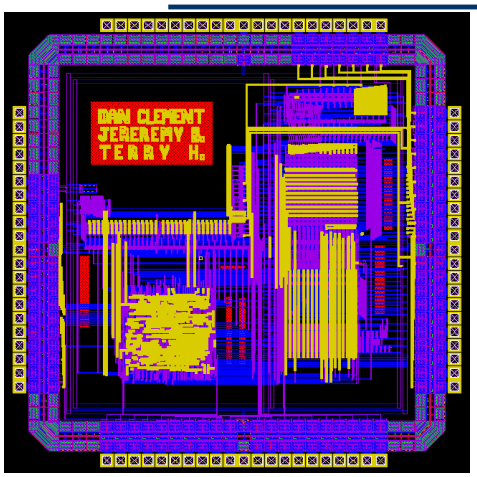


Zoom In…



A Hair (100 microns)

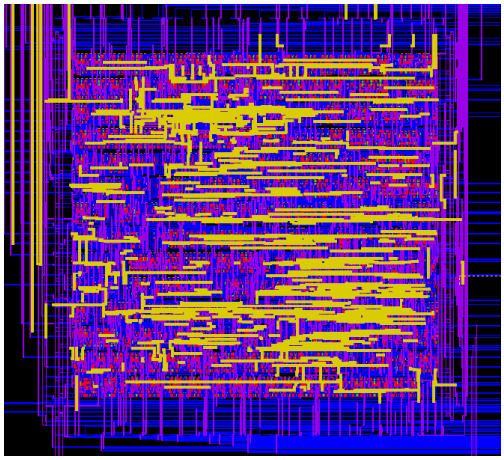
Another Class Project (2001)



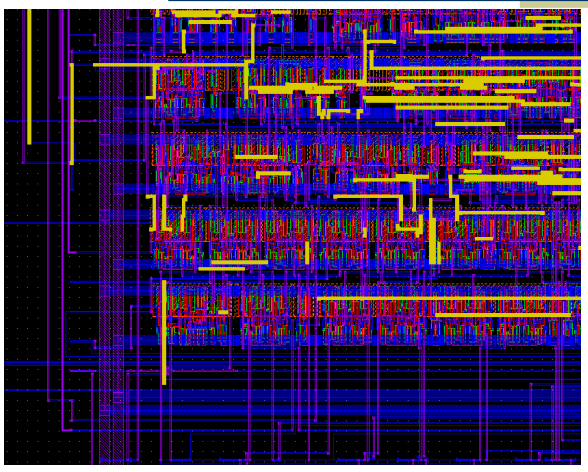
3.0mm x 3.0mm

84 I/O Pads

Standard-Cell Part



Standard-Cell Zoom



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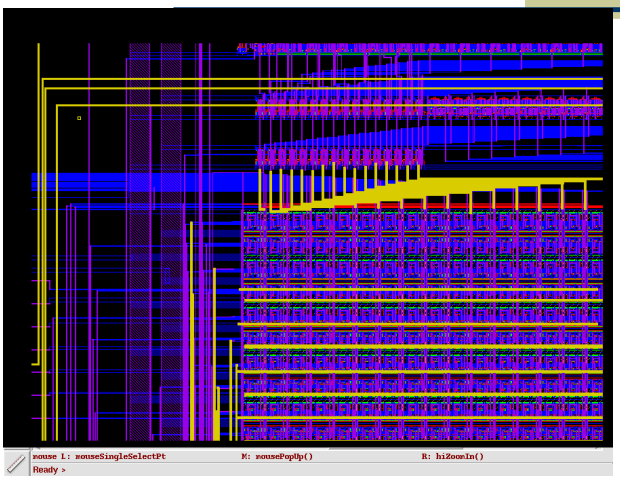
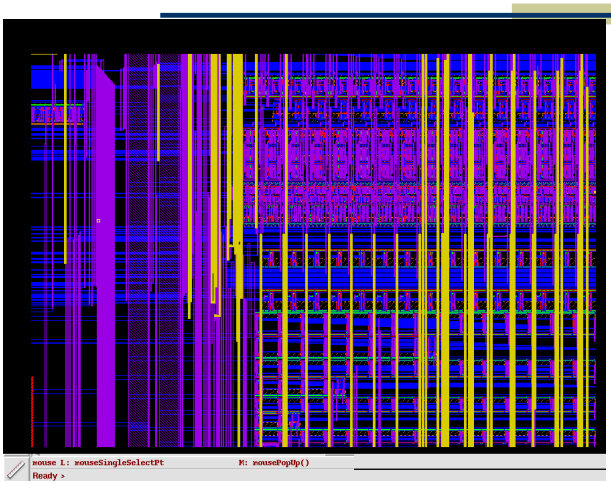
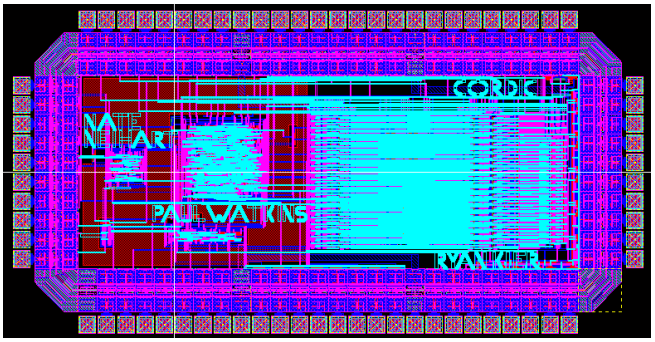


Adder/Shifter

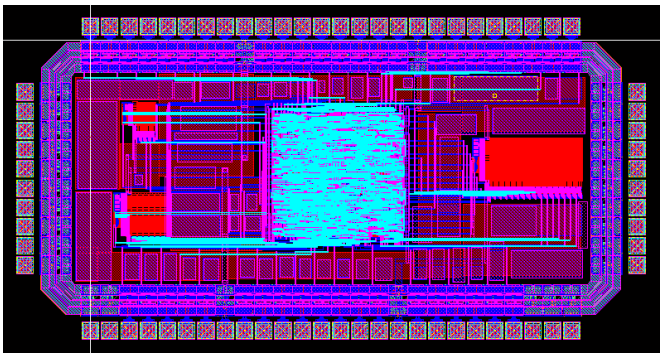


Class project from 2002



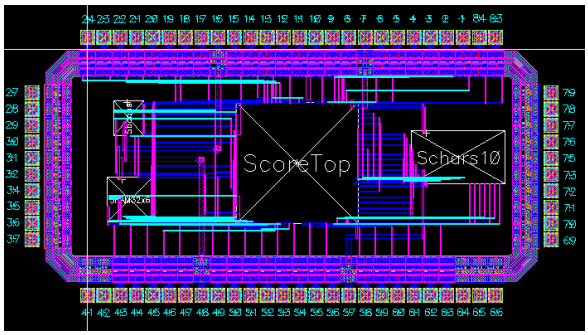
16-bit CORDIC Processor

Class project from 2003



Basketball Scoreboard Display

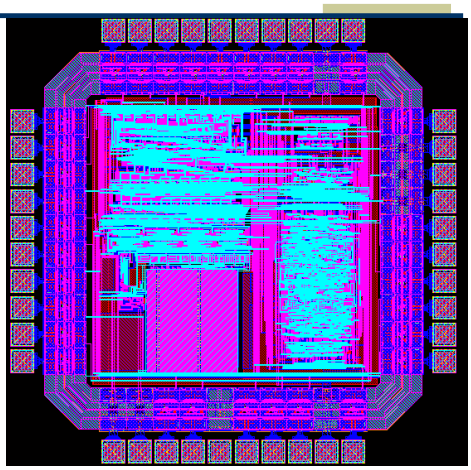
Class project from 2003



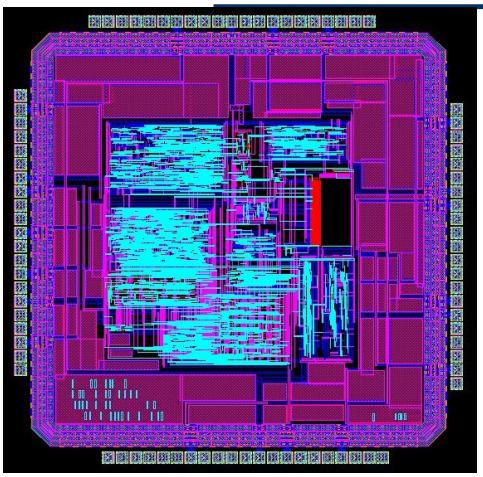
Basketball Scoreboard Display

Another class project (2003)

Simple processor (+, -, *, /) with ADC on the input



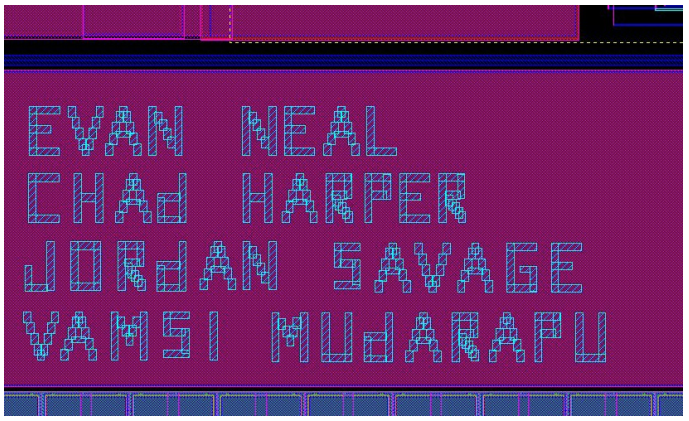
Class project from 2005



Bomb game With VGA output

Bomb game from 2005

Bomb game from 2005



Fabricate and Test the Chip

- We can fabricate the chips through MOSIS
  - Educational program sponsored by MOSIS' commercial activities
  - Chips are fabricated, packaged, and shipped back to us
- Then we get to test them to see what they do, or don't do…
  - ECE/CS 6712 in spring semester
  - Test hardware is Tektronix LV500

What Is "Design"?

- What is the design process?
- What makes a good design?
- What are the skills required?

- This is part of what makes this a fun career!
  - We'll discuss this during the class

First Taste of VLSI

- This class gives broad coverage from transistors through design and implementation
- But... it leaves many holes in
  - Knowledge
  - Full tool flow
  - Best practice
  - Modern issues
- **6770 next semester fills gaps**

VLSI at Utah

- VLSI is a means to an end, not an end in itself...
  - How to build ultra small efficient systems
  - Pervasive in use and application areas
- My group performs significant VLSI research
  - Supported by NSF, Semiconductor Research Corp, plus directly from TI, Intel, Synopsys, Mentor Graphics, etc.
  - Methods of reducing power by 300% and increasing performance by 150%
  - Talk to me if you want more information

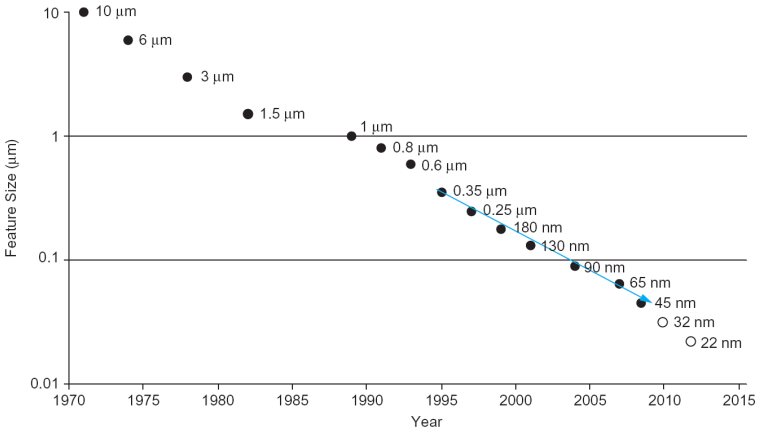
VLSI in industry

- Many career opportunities in VLSI
  - Varied skills needed
    - Architecture, CAD, design, validation, …
    - Software skills as critical as circuit skills
      - If you're a CS student, don't be intimidated!
  - Varied employment opportunities
    - Can work in large companies, small startups, etc.
      - I came here from Intel Research Labs 9 years ago
      - I am creating a small startup in this area
    - Graduate degree is highly valued here
      - Particularly for design side employment

IC Technology

- We'll use (oooold) the ON Semiconductor 0.5u 3-level-metal CMOS process
  - We have technology files that define the process
    - MOSIS Scalable CMOS Rev. 8 (SCMOS)
  - Tech files from NCSU CDK
    - NCSU toolkit is designed for custom VLSI layout
    - Design Rule Check (DRC) rules
    - Layout vs. Schematic (LVS) rules

IC Technology Curve



Big Picture for Course

- Start with transistors as switches
  - Boolean gates
- Study logical & electrical transistor behavior
- Mask layout for the gates
  - Design and characterize a set of gates
- Use the gates to build a whole-chip project
- Fabricate the chip and test in Spring 2015
  - This is optional
  - Rewarded with fun 1-hour testing class 6712

Class Project Details

- Standard Cell Library
  - Each group will design a small, but useful, standard cell library
    - Use HDL synthesis with this library as a target
    - Use Cadence SOC Encounter for place and route
- Custom Datapath
  - Use ICC router to connect HDL-Synthesized control to custom-designed datapath
  - It will be VERY helpful to have a mix of knowledge on your team

Class Project Tools

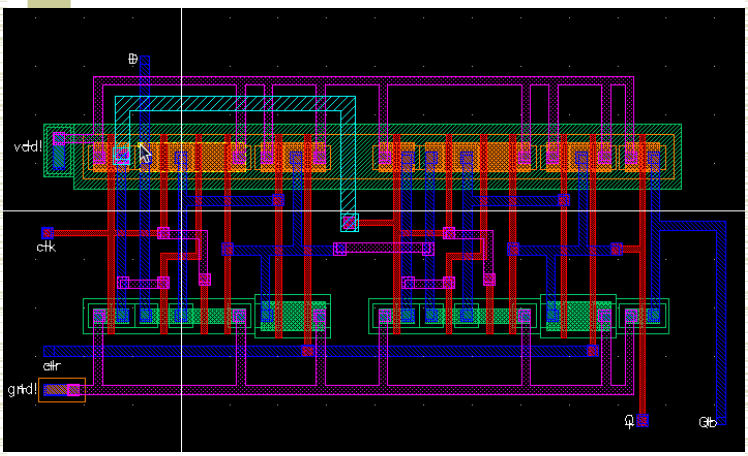
- Multiple design views for your library cells:
  - Start with Schematic, Verilog, Symbol, Layout views of each cell
  - Complete design in Composer schematics, simulated with Verilog
  - Complete design at layout level in Virtuoso with detailed simulation using Spectre
  - Validate they are the same with LVS
  - Custom layout for datapath
- Synthesized controller using Synopsys or Cadence RTL
- Place-Route with Encounter Digital Implementation System (EDI)
- Final assembly back in Virtuoso

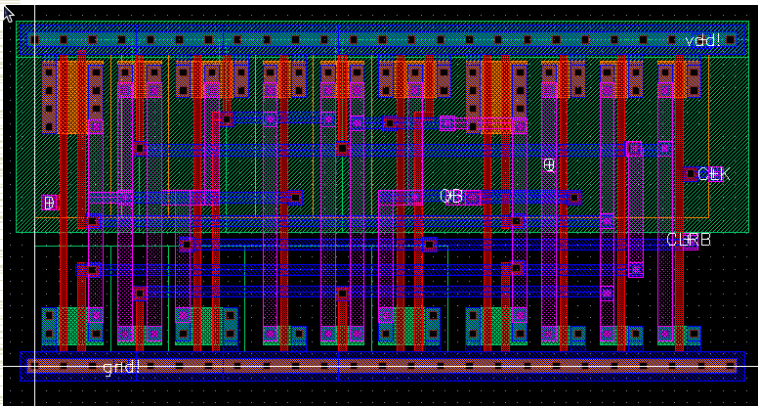
Timetable

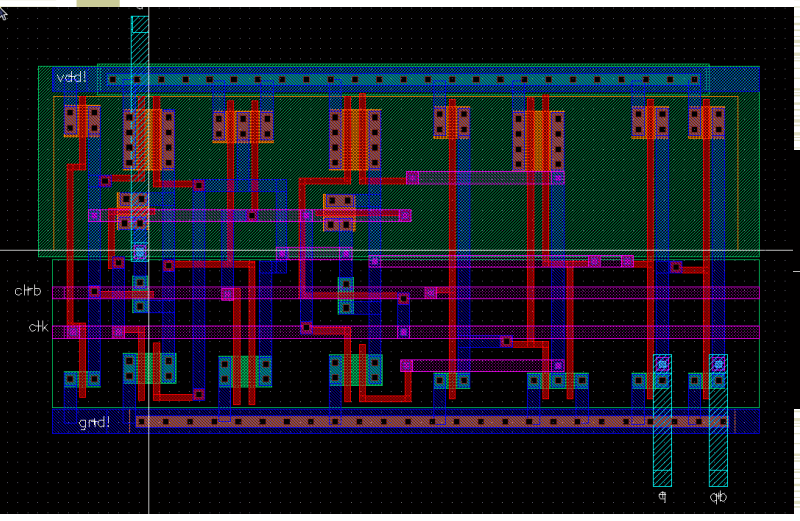
- This class/project will be a race to the finish!
  - There is no slack in this schedule!!!
- *VLSI design always takes longer than you think*
  - Even if you take that rule into account!
- *After you have 90% finished, there's only 90% left…*
  - All team members will have to contribute!
    - Team peer evaluations twice a semester

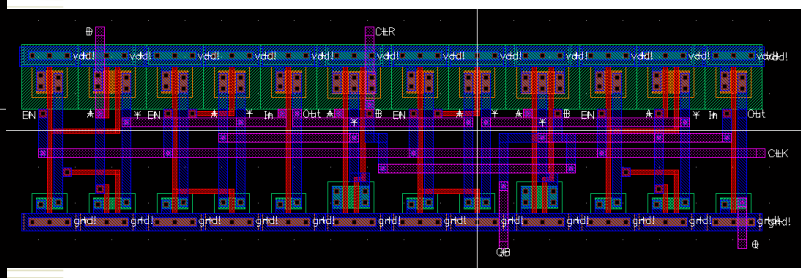
Layout Examples - DFF

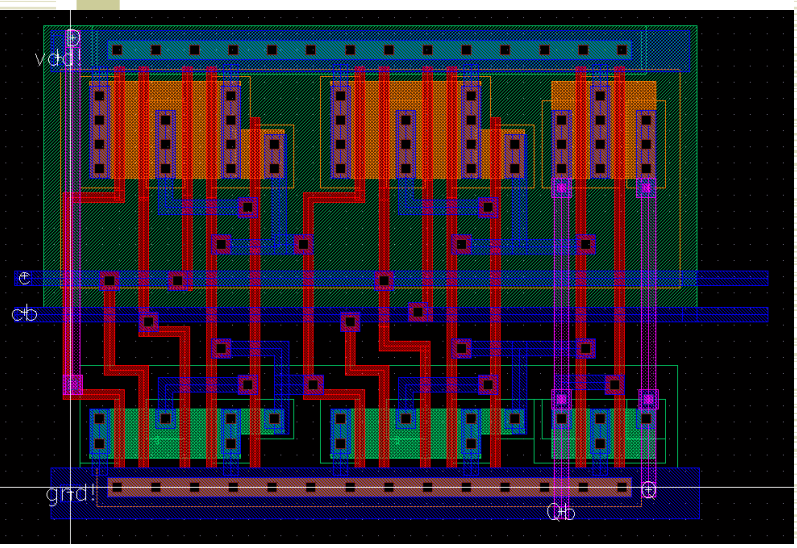
- Student designs from 2009
- Not exactly the same circuit, but pretty close
- Which ones are better designed than others?

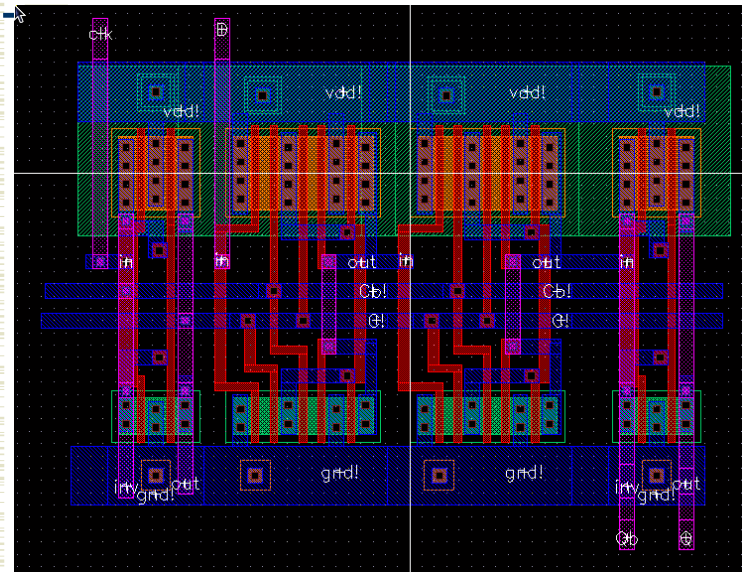


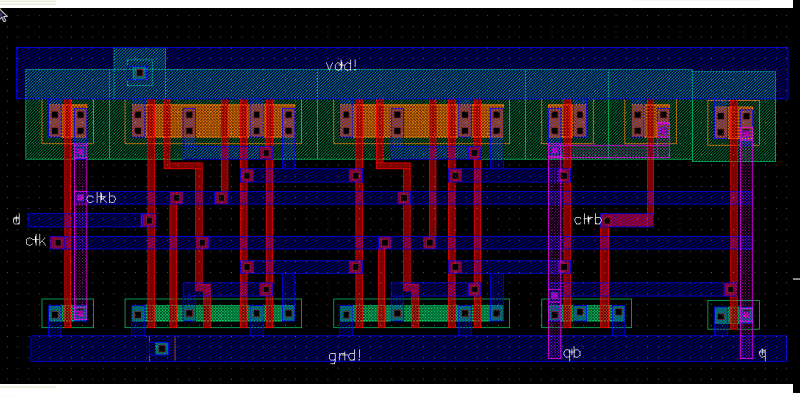


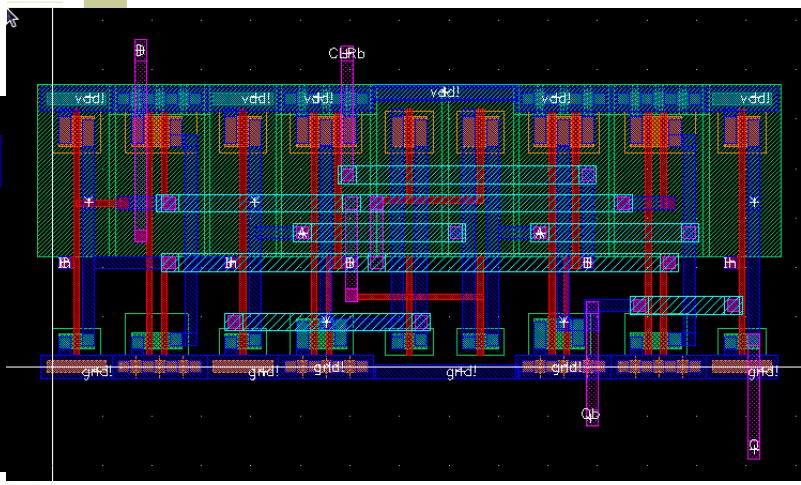


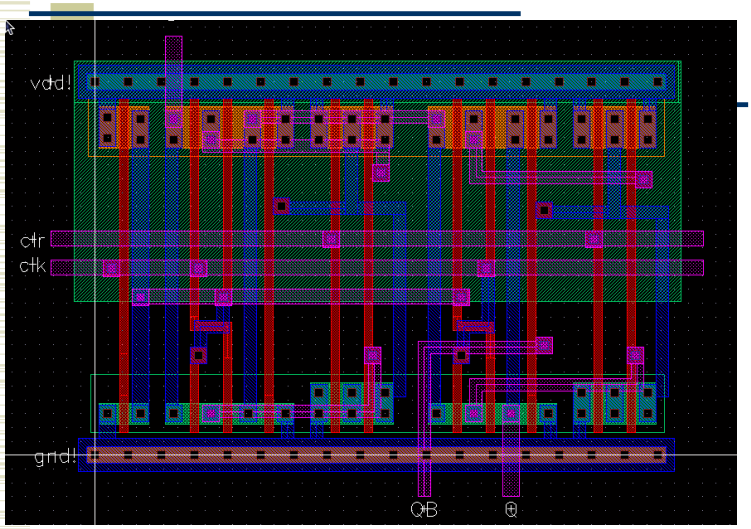


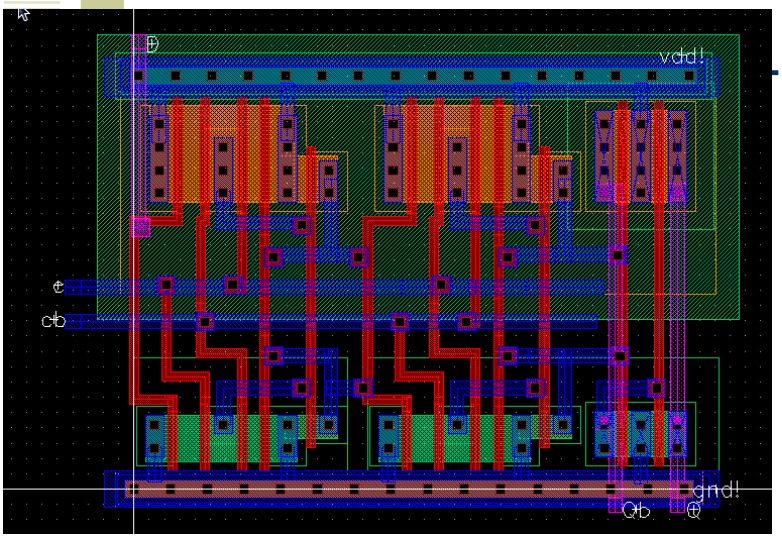

vdd!
ctb
grnd!
Qb

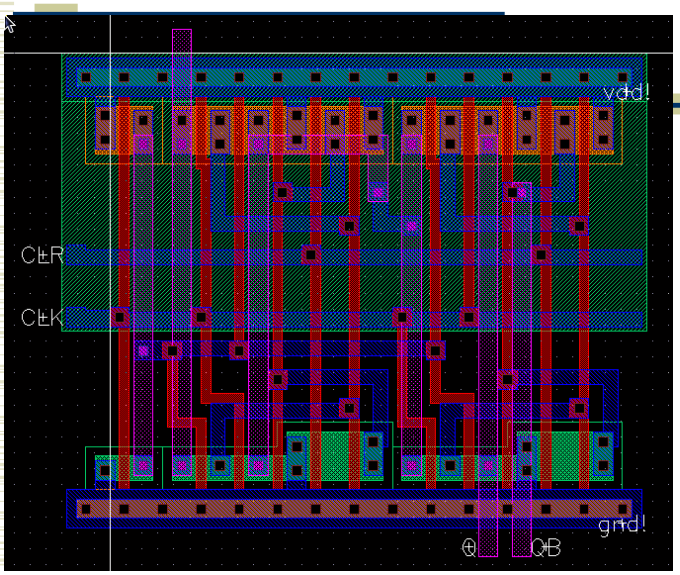

ctk
vdd!
vdd!
vdd!
vdd!
in
in
out
in
out
in
Ctb!
Ct!
Ctb!
Ct!
inv
grnd!
out
grnd!
grnd!
inv
grnd!
out
Qb

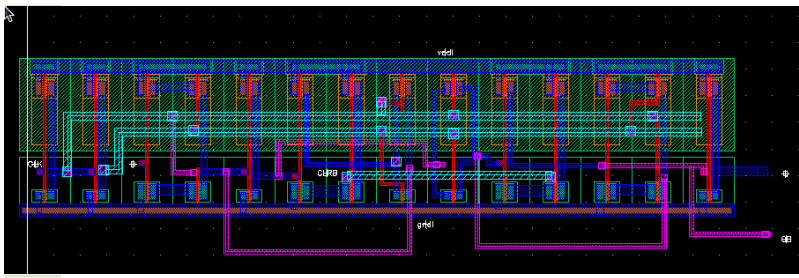

vdd!
ctkb
ctk
ctrb
grnd!
qb
q

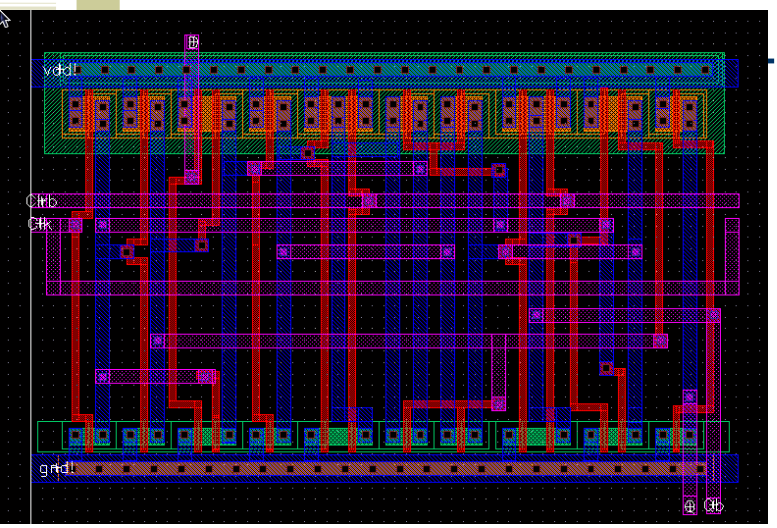

CtRb
vdd!
vdd!
vdd!
vdd!
vdd!
vdd!
in
in
in
in
grnd!
grnd!
grnd!
grnd!
grnd!
grnd!
Qb
q

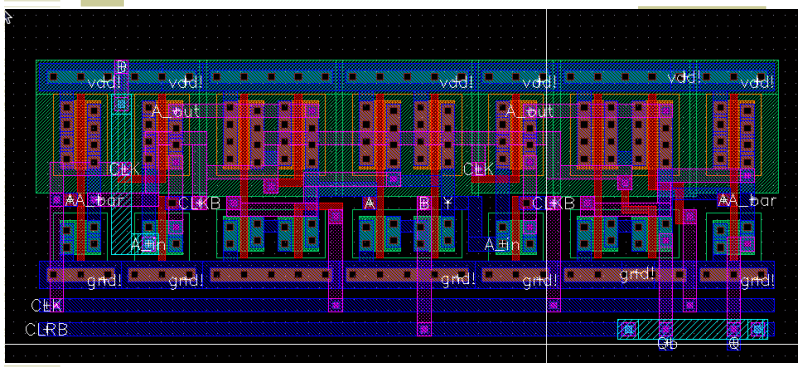

vdd!
ctr
ctk
grnd!
QB
Q

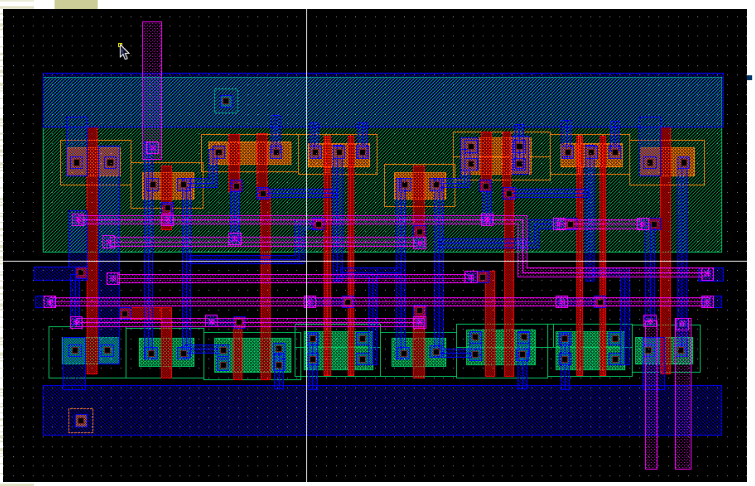

vdd!
ctb
grnd!
Qb
Q

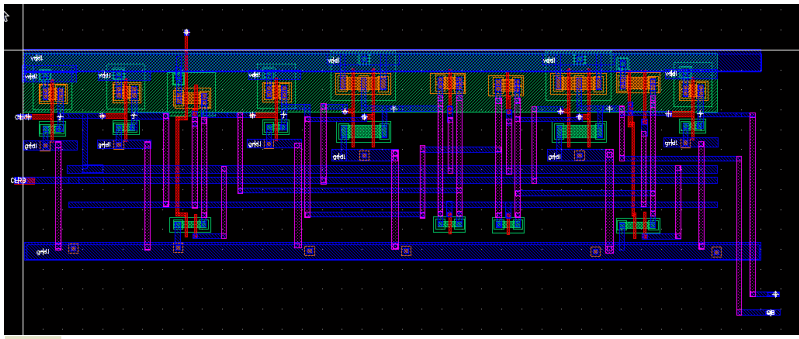

vdd!
CLR
CLK
gnd!
Q
QB

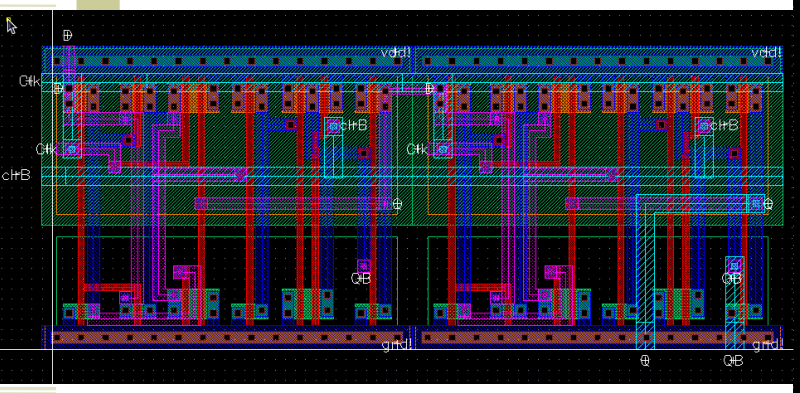


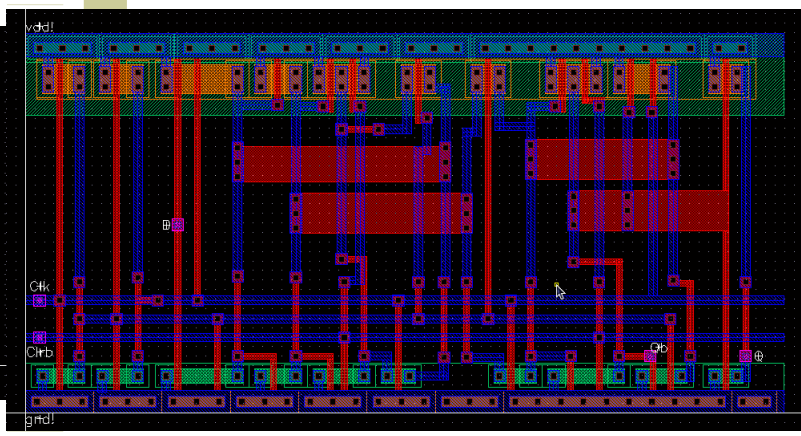

vdd!
CLRB
CLK
gnd!
Q
QB


vdd!
A_out
CLK
AA_bar
CLKB
A
B
Y
Ain
gnd!
CLK
CLRB
Q
QB









Class Summary

- Learn about VLSI design
  - Develop tool & layout skills independently
  - Form a team – develop a cell library
  - Decide on an architecture
  - Use the library to make a chip implementing the architecture
    - Verilog / synthesis / place and route / chip fab

Electronics Summary

- Voltage is a measure of electrical potential energy
- Current is moving charge caused by voltage
- Resistance reduces current flow
  - Ohm's Law: $V = I R$
- Power is work over time
  - $P = V I = I^2R = V^2/R$
- Capacitors store charge
  - It takes time to charge/ discharge a capacitor
  - Time to charge/discharge is related exponentially to RC
  - It takes energy to charge a capacitor
  - Energy stored in a capacitor is $(1/2)CV^2$

Energy (joules): work required to move one coulomb of charge by one volt or work done to produce one watt for one sec

Reminder: Voltage Division

- Find the voltage across any series-connected resistors

$$V_X = \frac{R_X}{R_{tot}} V_S$$

Resistance of resistor X

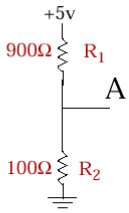
Voltage across resistor X

Total series resistance

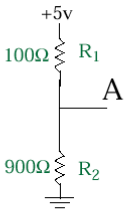
Total voltage

Example of Voltage Division

- Find the voltage at point A with respect to GND



$$V_X = \frac{R_X}{R_1 + R_2} V$$



Example of Voltage Division

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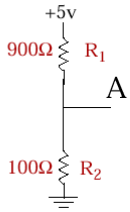
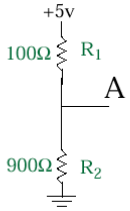


$$V_X = \frac{R_X}{R_1 + R_2} V$$

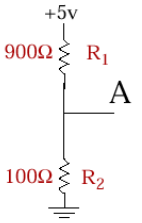


V_1 = (900/1000) 5v = 4.5v
V_2 = (100/1000) 5v = 0.5v
So, $V_{A\text{-}GND}$ = 0.5v

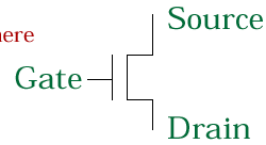
V_1 = (100/1000) 5v = 0.5v
V_2 = (900/1000) 5v = 4.5v
So, $V_{A\text{-}GND}$ = 4.5v

How Does This Relate to VLSI?

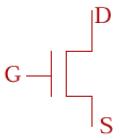
- Recall the voltage division example:
  - Consider what we could do if we had a device that we could switch from high resistance to low resistance
  - We could use it to force A high or low depending on the relative resistance of the elements



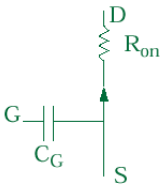
- This is a transistor
  - Specifically a CMOS FET
  - Complementary Metal-Oxide Semiconductor Field Effect Transistor
  - If voltage on Gate is high, then there is a low-resistance between Source and Drain, otherwise it's a very high-resistance



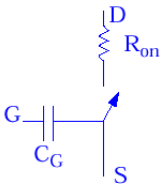
Model of a CMOS Transistor



Switch Level Model



Switch is closed if Gate voltage is high

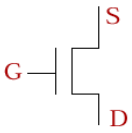


Switch is open if Gate voltage is low

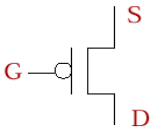
R_{on} = Some resistance in FET itself
C_G = Capacitance of the gate

Two Types of CMOS Transistors

- N-type transistor
  - High voltage on Gate connects Source to Drain
  - Passes 0 well, passes 1 poorly



- P-type transistor
  - Low voltage on Gate connects Source to Drain
  - Passes 1 well, passes 0 poorly

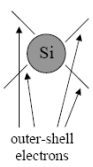


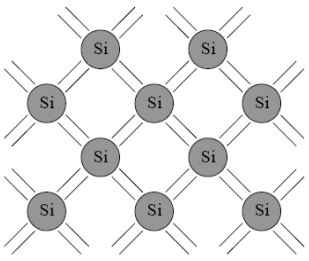
CMOS Transistors

- Complementary Metal Oxide Semiconductor
- Two types of transistors
  - Built on silicon substrate
  - "majority carrier" devices
  - Field-effect transistors
    - An electric field attracts carriers to form a conducting channel in the silicon…
    - We'll get much more of this later…
    - For now, just some basic abstractions

Silicon Lattice

- Transistors are built on a silicon substrate
- Silicon is a Group IV material
- Forms crystal lattice with bonds to four neighbors

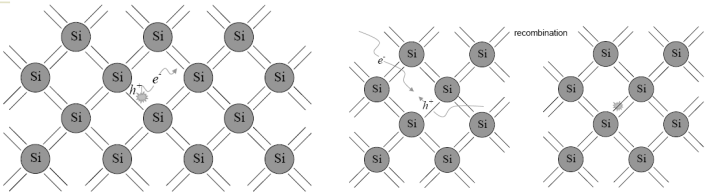




Figures from Reid Harrison

“Semi” conductor?

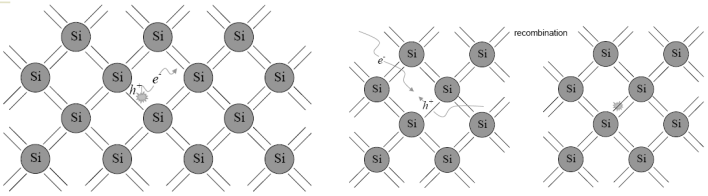
- Thermal energy (atomic-scale vibrations) can shake an electron loose
  - Leaves a “hole” behind



Figures from Reid Harrison

“Semi” conductor?

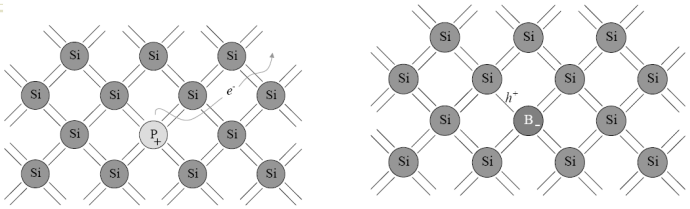
- Room temperature: 1.5×10^{10} free electrons per cubic centimeter
  - But, 5×10^{22} silicon atoms / cc
  - So, one out of every 3 trillion atoms has a missing e



Figures from Reid Harrison

Dopants

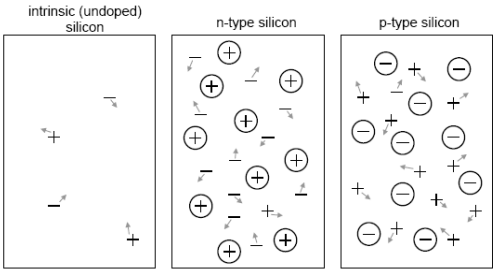
- Group V: extra electron (n-type)
  - Phosphorous, Arsenic,
- Group III: missing electron, (p-type)
  - Usually Boron



Figures from Reid Harrison

Dopants

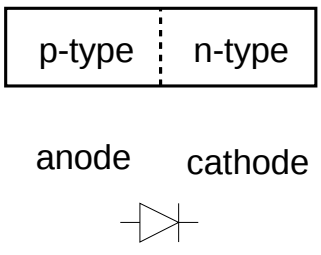
- Note that each type of doped silicon is electrostatically neutral in the large
  - Consists of mobile electrons and holes
  - And fixed charges (dopant atoms)



Figures from Reid Harrison

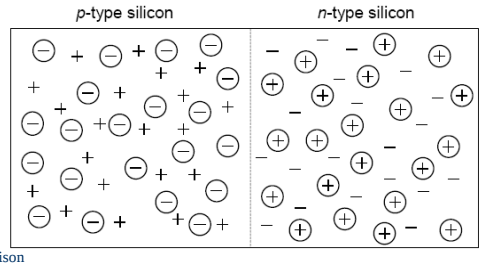
p-n Junctions

- A junction between p-type and n-type semiconductor forms a diode.
- Current flows only in one direction



p-n Junctions

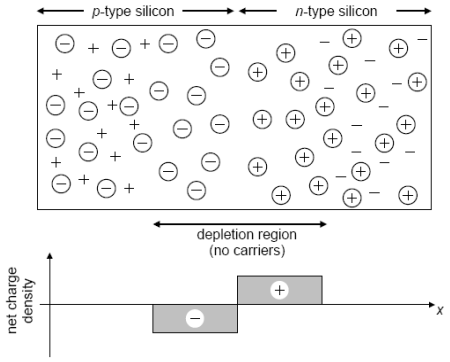
- Two mechanisms for carrier (hole or electron) motion
  - Drift - requires an electric field
  - Diffusion – requires a concentration gradient



Figures from Reid Harrison

p-n Junctions

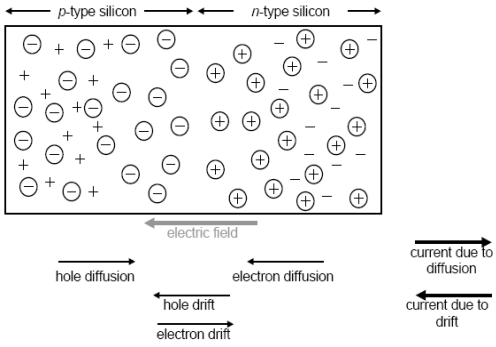
- With no external voltage diffusion causes a depletion region
  - Causes an electric field because of charge recombination
  - Causes drift current…



Figures from Reid Harrison

p-n Junctions

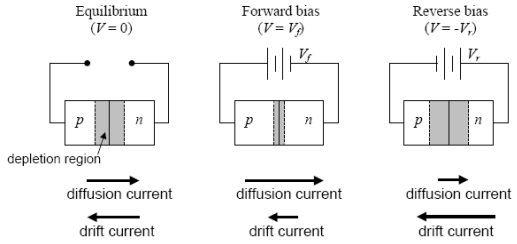
- Eventually reaches equilibrium where diffusion current offsets drift current



Figures from Reid Harrison

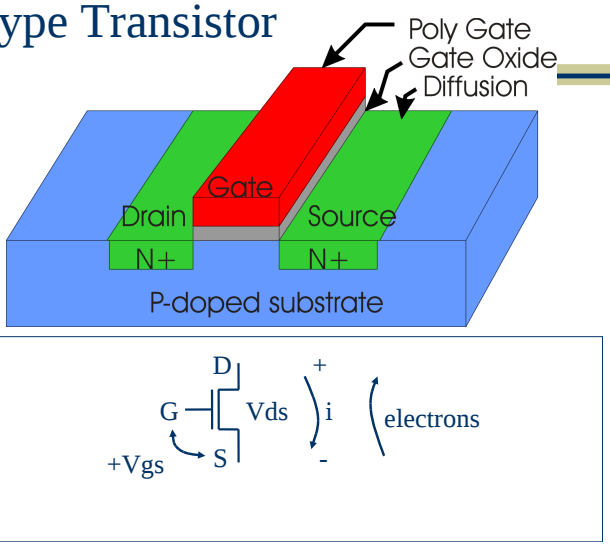
p-n Junctions

- By applying an external voltage you can modulate the width of the depletion region and cause diffusion or drift to dominate…



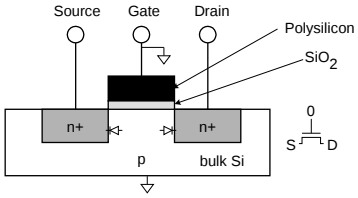
Figures from Reid Harrison

N-type Transistor



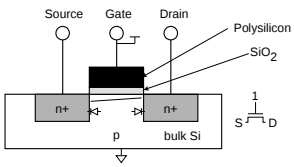
nMOS Operation

- Body is commonly tied to ground (0 V)
- When the gate is at a low voltage:
  - P-type body is at low voltage
  - Source-body and drain-body diodes are OFF
  - No current flows, transistor is OFF

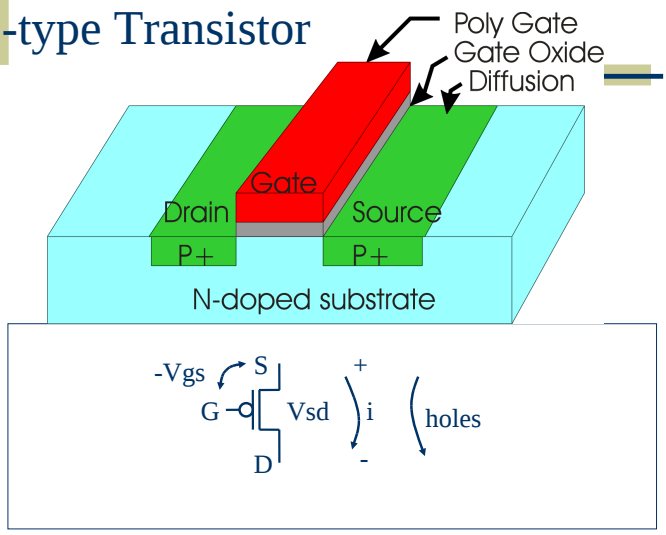


nMOS Operation Cont.

- When the gate is at a high voltage:
  - Positive charge on gate of MOS capacitor
  - Negative charge attracted to body
  - Inverts a channel under gate to n-type
  - Now current can flow through n-type silicon from source through channel to drain, transistor is ON

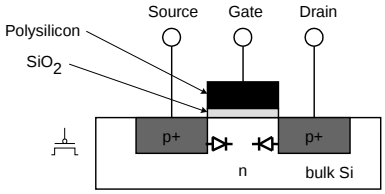


P-type Transistor



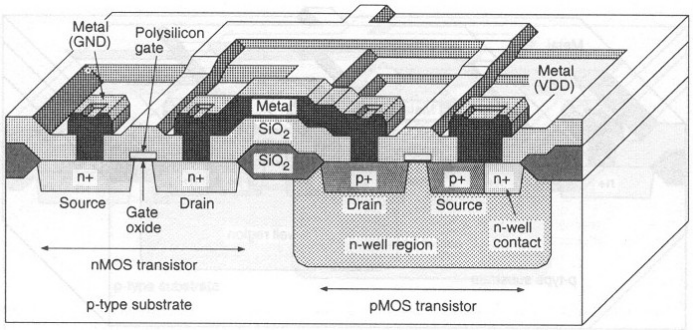
pMOS Transistor

- Similar, but doping and voltages reversed
  - Body tied to high voltage (V_{DD})
  - Gate low: transistor ON
  - Gate high: transistor OFF
  - Bubble indicates inverted behavior



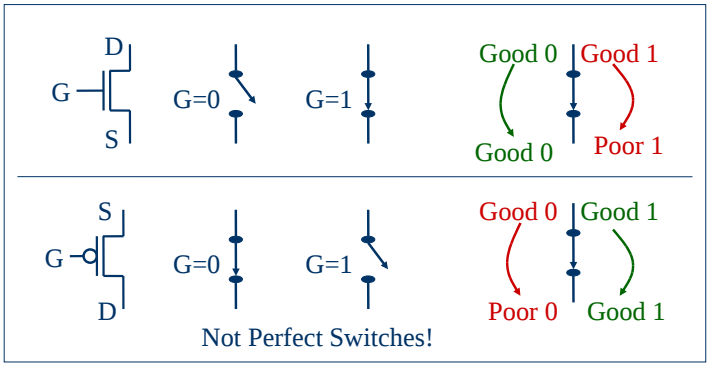
A Cutaway View

- CMOS structure with both transistor types



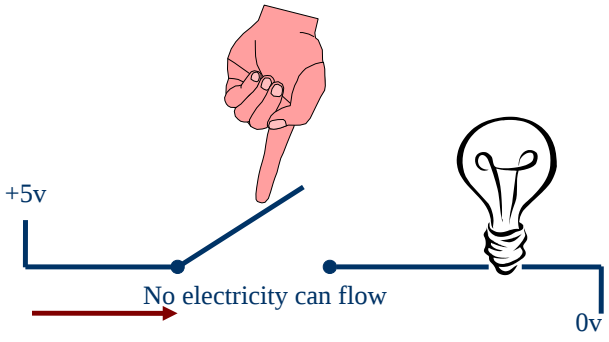
Transistors as Switches

- For now, we'll abstract away most analog details…



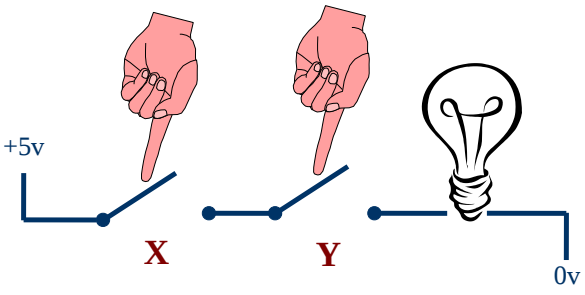
"Switching Circuit"

- For example, a switch can control when a light comes on or off



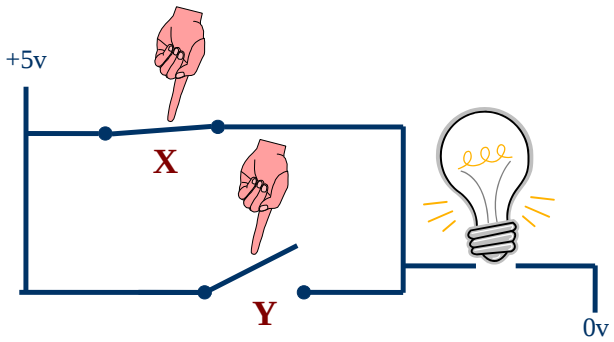
"AND" Circuit

- Both switch **X** **AND** switch **Y** need to be closed for the light to light up



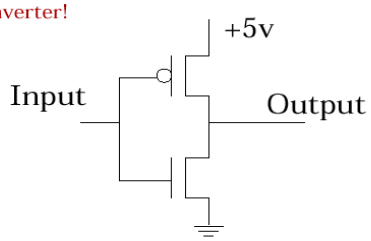
"OR" Circuit

- The light comes on if either **X OR Y** are closed



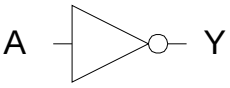
CMOS Inverter

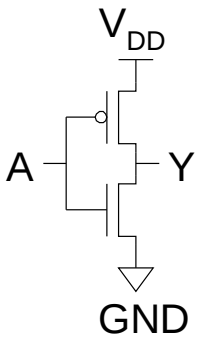
- Consider this connection of transistors
  - If input is at a high voltage, output is low
  - If input is at a low voltage, output is high
- By changing the resistances, it becomes one of two different voltage dividers
  - It's a voltage inverter!



CMOS Inverter

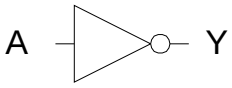
A	Y
0	
1	

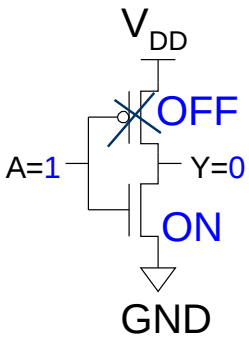




CMOS Inverter

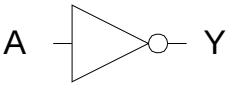
A	Y
0	
1	**0**

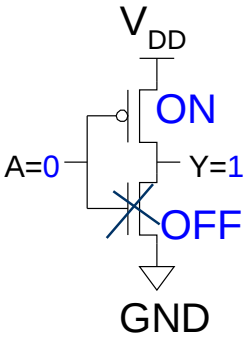




CMOS Inverter

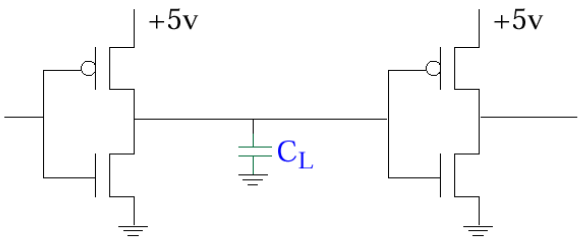
A	Y
0	**1**
1	0





Timing Issues in CMOS

- Recall that it takes time to charge capacitors
- Recall that the gate of a transistor looks like a capacitor
- Wires have resistance and capacitance also!

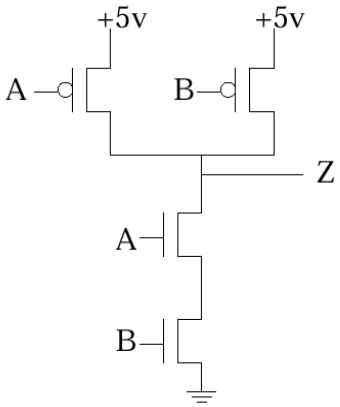


Power Consumption

- Power is consumed in CMOS by charging and discharging capacitors
  - Note that there no static power dissipation in CMOS
  - There's never a DC path to ground
- Good news:
  - You're not consuming power unless you're switching
- Bad news:
  - Switching activity is caused by clock, which is going faster and faster
- If the first-order power effect is capacitor charging/discharging, and the clock causes this:

$$P = C V^2 f$$

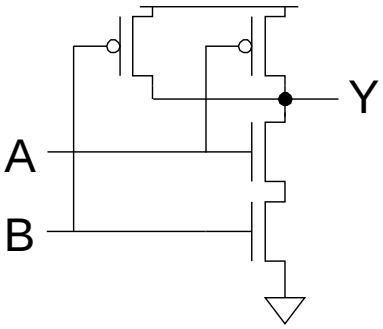
CMOS NAND Gate

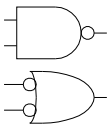


A	B	Z
0	0	1
0	1	1
1	0	1
1	1	0

CMOS NAND Gate

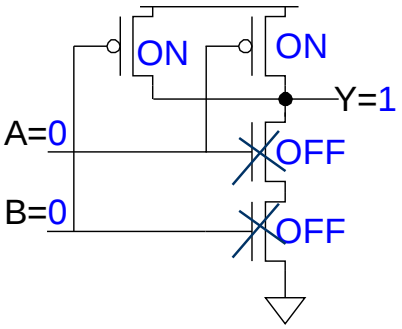
A	B	Y
0	0	
0	1	
1	0	
1	1	

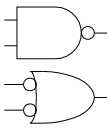




CMOS NAND Gate

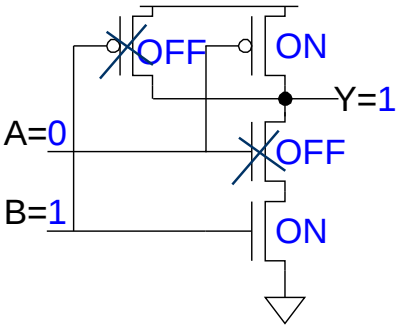
A	B	Y
0	**0**	**1**
0	1	
1	0	
1	1	

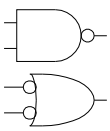




CMOS NAND Gate

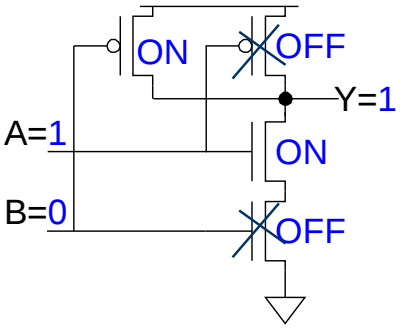
A	B	Y
0	0	1
0	**1**	**1**
1	0	
1	1	

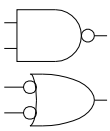




CMOS NAND Gate

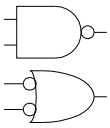
A	B	Y
0	0	1
0	1	1
1	**0**	**1**
1	1	

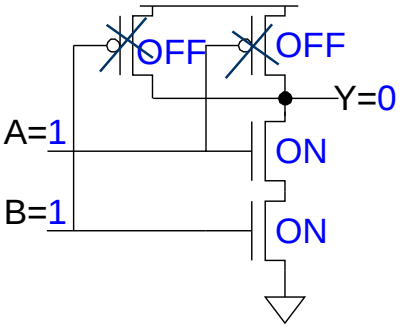




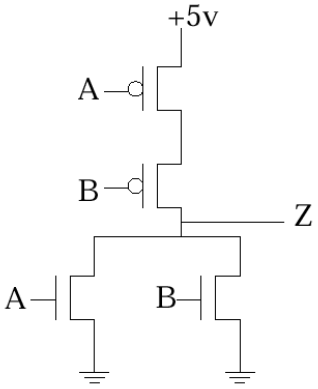
CMOS NAND Gate

A	B	Y
0	0	1
0	1	1
1	0	1
1	**1**	**0**

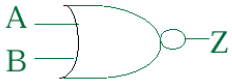




CMOS NOR Gate



A B	Z
00	1
01	0
10	0
11	0

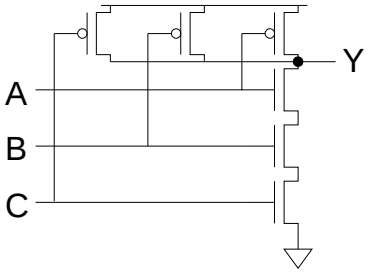


3-input NAND Gate

- Y pulls low if ALL inputs are 1
- Y pulls high if ANY input is 0

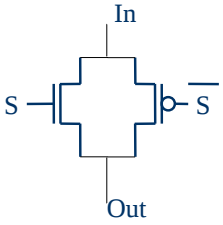
3-input NAND Gate

- Y pulls low if ALL inputs are 1
- Y pulls high if ANY input is 0



N-type and P-type Uses

- Because of the imperfect nature of the the transistor switches
  - ALWAYS use N-type to pull low
  - ALWAYS use P-type to pull high
  - If you need to pull both ways, use them both



S=0, In ≠ Out

S=1, In = Out

Switch to Chalkboard

- Complex Gate
- Tri-State
- Latch
- D-register
- XOR