ECE/CS 5710/6710 – Digital VLSI Design
Lab Assignment #2

Due Tuesday Sept. 23rd via canvas

1 Introduction

In this laboratory assignment you will start physical design. You will implement a schematic and the physical design that implements the same functionality as the schematic. Physical design is an exacting task, and you ALWAYS need to verify that your layout is correct. You will then use two software tools to verify the correctness of your physical design. Design rule checking (DRC) software ensures that your layout obeys the myriad set of design rules. The physical design will then be structurally verified against the schematic (used as the specification). This is accomplished with the layout versus schematics (LVS) software. You will then run SPICE simulation to generate analog waveforms of your design.

2 Assignment

Following are the tasks which you will need to complete for this Lab.

1. Design an inverter using transistors in a Composer schematic and simulate the inverter with **Verilog** *and* using SPICE (the Analog Environment) with **Spectre**. (This is covered in Chapters 3, 4, and 7 in *Design with Cadence and Synopsys*.) Create a symbol view for this inverter. You may want to do this assignment within your lab1 library that you created in lab assignment #1 rather than create a new library. You can use nmos, pmos, vdd, and gnd devices from either the `NCSU_Analog_Parts` or `UofU_Analog_Parts` libraries. The difference (as described in Chapter 3) is that the NCSU devices have zero delay when simulated by Verilog simulators, whereas the UofU devices have 100ps of delay. SPICE simulation (Spectre) uses transistor models that provide precise delays based on device sizes, loads, and parasitic capacitances. This simulator produces results with analog waveforms. Set the width of the devices in this inverter to be 1.5μ (1.5 microns, also 5 λ) for the nmos and 3μ (3 microns, also 10 λ) for the pmos. This will be our "unit sized" (minimum size) inverter for all design we do in class. Set the widths when you put the transistors in the schematic or use the `q` properties button to change parameters of transistors that are already in your schematic. The transistor length should be the default (600n which is 600nm or 0.6 microns or 2 λ).

2. Draw the layout for the inverter in Virtuoso (covered in Chapter 5 of *Design with Cadence and Synopsys*). For this layout, and for the NAND gate in assignment task 3, you don't have to use the standard cell template in Chapter 6, but you should think about making the two layouts compatible in terms of (at least) the vdd and gnd connections. Run DRC and LVS to make sure you met the design rules, and that your layout does correspond to the transistor schematic in assignment task 1. Extract and simulate this inverter with Spectre (i.e. simulate the extracted view). Compare the waveform to the analog waveform from task 1. Note that you should draw the layout of the transistors to match the widths you used in the schematic.

3. Draw a layout for the two-input NAND gate that you designed in Lab Assignment #1. Simulate that layout using Spectre (SPICE simulation using the extracted view) and compare against the Verilog simulation from Lab Assignment #1. Verify the NAND gate layout with DRC and LVS against the transistor version from Lab Assignment #1. The transistor widths you should use are 3μ for both nmos and pmos. (Why did we pick these widths?) Update the schematic to match these widths.

4. Use the layout of the NAND gate and the layout of the inverter to design the layout version of the function from Lab Assignment #1 in Virtuoso. Modify the schematic for the function to use the inverter and NAND instead of only NAND gates. Remember that the function you're implementing is:

$$F = \overline{a}\overline{b} + \overline{a}c + \overline{b}c \tag{1}$$

   In the layout you should include instances of the layout for the NAND and layout for the inverter in a new layout view, make the connections by drawing layout to connect them. Remember to connect vdd and gnd as well as the signals. Simulate this layout in Spectre. Verify with DRC and LVS against the modified schematic.

3 Instructions

Note that the layout versus schematic (LVS) verification software will not successfully run unless you have already successfully run the design rule checking (DRC) software. Thus, you don't need to hand in the DRC results. You can get the LVS logs in two ways:

1. In the LVS window after you finish the LVS step, you need to press the `output` button to view the LVS log. In the LVS log window, click on the `File | save as` drop-down menu and save it to a file.

2. A log file is generated every time you run the LVS tool called `si.out`. This file can be found in your `IC_CAD/5710/LVS` directory.

4 Deliverables

Create a tar file containing all deliverables and upload it to canvas.
For your inverter, NAND gate, and function F, include:

1. an `xv` image of
   (a) schematics
   (b) layout
   (c) verilog simulation results
   (d) analog SPICE simulations from Spectre
2. the files containing
   (a) verilog simulation testbenches
   (b) LVS logs