ECE/CS 5710/6710 – Digital VLSI Design
Lab Assignment #4

Due Tue. Oct. 20th via canvas

1 Introduction

In this lab you will explore the DC characteristics of gates and some power and delay properties of collections of transistors. This material is covered in the Weste and Harris textbook in Chapters 2 and 4. A small homework assignment from the textbook will also be assigned. This will allow you to practice some of the design and modeling principles discussed in lectures.

2 Background

The SPICE simulations you have been running in Cadence's Spectre have been using *transient analysis* to plot how a waveform changes across time. In this simulation mode the results of applying time varying signals to the circuit are observed. The waveforms produced by this simulation mode are generally what digital designers are most interested in since it provides data on delays, power, rise and fall times, etc. of a circuit.

However, another important aspect of circuit design is to observe the behavior of the devices themselves. This can be accomplished by applying *DC analysis* that reports on the steady state, rather than the time-varying state, of a circuit. For example, Figure 2.7 in your text is a plot of steady state behavior of an nMOS transistor mapping the I_{ds} current as V_{ds} is changed. In fact, there are five different DC analyses in this figure. Each of the five curves is a DC analysis that holds the V_{gs} at a fixed level, then sweeps the V_{ds} from 0v to 5v and plots the resulting I_{ds}.

3 Instructions

Chapter 7, Section 7.5 in *Design with Cadence and Synopsys* describes how to run exactly the same SPICE simulations as the textbook in Spectre.

4 Assignment

The following tasks are required for this lab:

1. Run a parametric DC analysis of a single nmos device as described in Design with Cadence and Synopsys. The nmos device should have 1.5μ width with a 0.6μ channel length. Plot the results. Use five curves with V_{gs} at 1, 2, 3 , 4, and 5 volts.
2. Run a similar parametric DC analysis of the same nmos device but make it 6μ wide and 0.6μ long. Plot the results with the same five voltages as above.
3. Use DC analysis to plot the switching point of a standard inverter. See Figure 2.27 in your textbook for an example. The inverter should be a $2\times$ inverter with an nmos device 3μ wide and a pmos device 6μ wide. Connect the input of the inverter to a DC voltage source and sweep the DC voltage from 0 to 5 volts for the DC analysis. Plot the output voltage.
4. Now change the width of the pmos from 1.5μ to 7.5μ in five equal steps. You can change the size by modifying the width field of the pmos device. Run a parametric DC analysis for each width sweeping the input from 0v to 5V. See Figure 2.28 in your text for an example.
5. Solve the following problems from your textbook: 1.2, 1.6, 1.7, 1.9, 1.10, 1.16 (a,b,c only), 1.18 (a,b only), 2.4, 2.9, 2.11, 2.20, 2.21.

5 Deliverables

Include the following deliverables in a tar file for this lab:

1. A README file describing the files and any issues you had with the lab.
2. Scan your work into a file that contains the result of the nine problems from the textbook, 1.2, 1.6, 1.7, 1.9, 1.10, 1.16 (a,b,c only), 1.18 (a,b only), 2.4, 2.9, 2.11, 2.20, 2.21.
3. The schematic and plot for the DC analysis of the 1.5μ nmos device.
4. The DC plot and schematic of the 6μ wide nmos device. Report how the I_{ds} currents compare to the 1.5μ wide device.
5. The schematic and DC plot of the inverter.
6. The plot of the inverter with five different pmos sizes. Report which size results in a switching point closest to $\frac{V_{dd}}{2}$.