Lab 5

- Designing the first five cells in your library
  - Multiple cell views
- ELC library characterizer
- Abstract generator
- Synopsys database generation
  - Using the cells in synthesis

CS/ECE 6710 Tool Suite
- Synopsys Design Compiler
- Verilog sim
- Behavioral Verilog
- Synopsys Database Generation

Start with Cells
- Layout View
- Schematic View
- Symbol View
Behavioral View

```verilog
module NAND2X1 (Y, A, B);
  output Y;
  input A;
  input B;
  always @ (A or B)
    if (A) Y <= 1;
    else if (B) Y <= 1;
  endmodule
```

Single Schematic with All Cells

Create Netlist of that Cell

```sh
sp2elc foo.scs dut.scs
```

Convert to ELC format

```sh
sp2elc foo.scs dut.scs
```
Run ELC

- Encounter Library Characterizer
  - Figures out what each cell is (logic)
  - Generates test inputs for Spectre
  - Runs Spectre
  - Checks output and extracts timings
  - Formats the output in .alf format

Results from ELC step 1

```
elc> db_gate
DESIGN : INVX1
NOT ( Y, A );
```

Results from ELC step 2

```
elc> db_spice -s spectre -p typical -keep_log
DESIGN        PROCESS       #ID         STAGE    STATUS    IPDB
-------------+-------------+----------+----------+-----------+------------
INVX1          typical       D0000     VERIFICATE   PASS        foo
INVX1          typical       D0001     VERIFICATE   PASS        foo
NAND2X1        typical       D0000     VERIFICATE   PASS        foo
NAND2X1        typical       D0001     VERIFICATE   PASS        foo
NAND2X1        typical       D0002     VERIFICATE   PASS        foo
NAND2X1        typical       D0003     VERIFICATE   PASS        foo
NAND2X1        typical       D0004     VERIFICATE   PASS        foo
NAND2X1        typical       D0005     VERIFICATE   PASS        foo
NAND2X1        typical       D0006     VERIFICATE   PASS        foo
NAND2X1        typical       D0007     VERIFICATE   PASS        foo
NOR2X1         typical       D0000     VERIFICATE   PASS        foo
NOR2X1         typical       D0001     VERIFICATE   PASS        foo
NOR2X1         typical       D0002     VERIFICATE   PASS        foo
```

Lots of text missing from these highlights...
Results from ELC step2

- Total Simulation : 20
- Total Passed     : 20(100.00%)
- Total Failed     : 0(0.00%)

Results from ELC step3

elc> db_output -report foo.alf.rep -alf foo.alf -p typical
NAND2X1        typical   2013-10-10 13:55:23 (2013-10-10 19:55:23 GMT) 8 (100%)
NORX1          typical   2013-10-10 13:55:23 (2013-10-10 19:55:23 GMT) 8 (100%)
elc> db_verilog -r foo.v
Reading : foo.ipdb/INVX1.design

Changing Names

- The ELC scripts make a library named “foo”
- Probably good to rename it Lib6710_00
  - Rename foo.lib to Lib6710_00.lib
  - You have to modify the library name inside the .lib file
  - Rename foo.v to Lib6710_00.v
  - You generate Lib6710_00.db from Lib6710_00.lib

Changing foo.lib to Lib6710_00.lib

```
CELL INVX1:
  now reading
  now converting
  ***** successful *****
CELL NAND2X1:
  now reading
  now converting
  ***** successful *****
CELL TIEHI:
  now reading
  now converting
  ***** successful *****
CELL TIELO:
  now reading
  now converting
  ***** successful *****
```

```
Total : 5 cells ( successful : 5  failed : 0 )
```

```
Changing foo.lib to Lib6710_00.lib
```

```
---
```
Converting .lib to .db

Using setup-synopsys from S13/F13
Assuming your OS is amd64
You are now set up to run the synopsys tools.

Working directory is /home/elb/VLSI/cadence-f13/ELC

Design Compiler Graphical
DC Ultra (TM)
Power Compiler (TM)
DesignWare (R)
DFT Compiler
Library Compiler (TM)

Version G-2012.06-SP3 for RHEL64 -- Oct 23, 2012
Copyright (c) 1988-2012 Synopsys, Inc.

Lots of text missing from these highlights…

Generating Abstract Views
Imported library in cad-abstract

Green checks are good!

Export Lib6710_00.lef file

"geometry lef"

Replace highlighted text with TechHeader.lef from class ELC directory

Final CAD5 Files…

- Nine views of every cell
  - abstract, abstract.ext, abstract.pin, analog_extracted, behavioral, cmos_sch, extracted, layout, symbol
  - DRC and LVS-checked, and simulated

- Four versions of the library description
  - Lib6710_00.lib
  - Lib6710_00.db
  - Lib6710_00.v
  - Lib6710_00.lef
**All Nine Views…**

Test with beh2str

- beh2str addsub.v addsub_dc.v Lib6710_00.db
- Results in addsub_dc.v and addsub_dc.v.rep

**addsub_dc.v**

```verilog
dmodule addsub ( a, b, addnsub, result );
  input [7:0] a;
  input [7:0] b;
  output [8:0] result;
  input addnsub;
  wire   n26, n27, n28, n29, n30, n31, n32, n33, n34, n35, n36, n37, n38, n39,
         n40, n41, n42, n43, n44, n45, n46, n47, n48, n49, n50, n51, n52, n53,
         n54, n55, n56, n57, n58, n59, n60, n61, n62, n63, n64, n65, n66, n67,
         ...;
  NAND2X1 U33 ( .A(n26), .B(n27), .Y(result[7]) );
  NAND2X1 U34 ( .A(b[7]), .B(n28), .Y(n27) );
  NAND2X1 U35 ( .A(n28), .B(n30), .Y(n29) );
  NOR2X1 U36 ( .A(n31), .B(n32), .Y(n29) );
  ...;
  NOR2X1 U216 ( .A(n188), .B(a[0]), .Y(n175) );
  NAND2X1 U217 ( .A(a[0]), .B(n188), .Y(n282) );
  INVX1 U218 ( .A(b[0]), .Y(n188) );
endmodule
```

**addsub_dc.v.rep**

```
Operating Conditions: typical   Library: Lib6710_00
Wire Load Model Mode: top
Startpoint: b[1] (input port)  
Endpoint: result[8] (output port)  
Path Group: (none)  
Path Type: max
Point                                    Incr       Path
------------------------------------------
input external delay                     0.00       0.00 r
b[1] (in)                                0.00       0.00 r
U198/Y (NOR2X1)                          0.50       0.50 f
U194/Y (NOR2X1)                          0.36       0.36 f
...                                      
U34/Y (NAND2X1)                          0.25      10.16 f
U33/Y (NAND2X1)                          0.24      10.40 r
result[8] (out)                          0.00      10.40 r
data arrival time                                  10.40
------------------------------------------
(Path is unconstrained)
```

**Summary**

- You now have a library that is fully functional
  - BUT – only on combinational circuits
  - No DFF yet!
- Every step of the way requires extreme care to get things exactly right
  - No trick to finding the right answer
  - The point is to practice working with the data & tools
Look ahead to EDI

Modify the Script Files

Placed and Routed Result