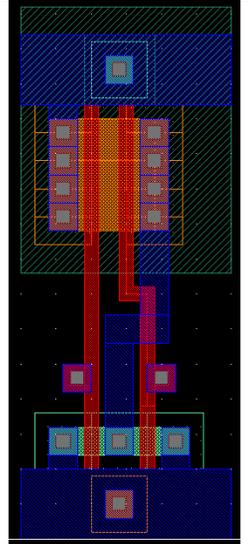


## Where are we?

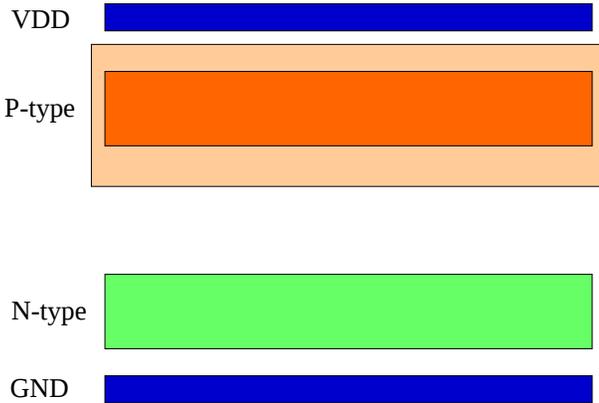
- ▶ Lots of Layout issues
  - ▶ Line of diffusion style
  - ▶ Power pitch
  - ▶ Bit-slice pitch
  - ▶ Routing strategies
  - ▶ Transistor sizing
  - ▶ Wire sizing

## Layout - Line of Diffusion

- ▶ Very common layout method
  - ▶ Start with a "line of diffusion" for each transistor type
  - ▶ Cross with poly to make transistors
  - ▶ This is the "type 2" NOR gate

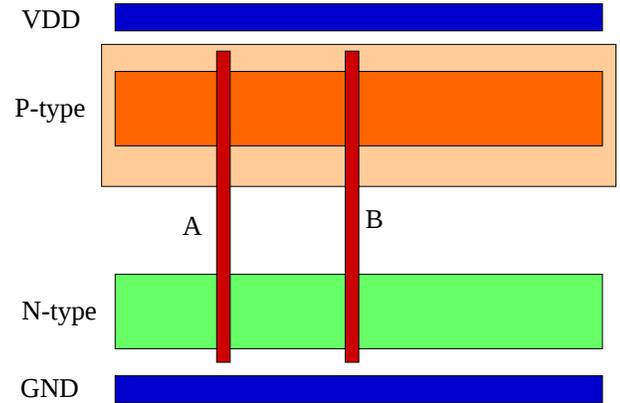


## Line of Diffusion in General



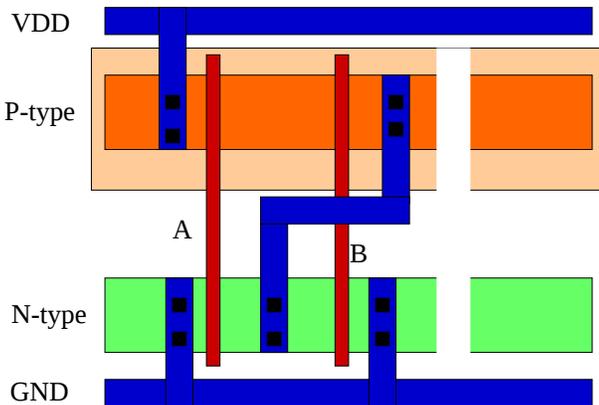
- ▶ Start with lines of diffusion for each transistor type

## Line of Diffusion in General



- ▶ Cross with Poly to make transistors

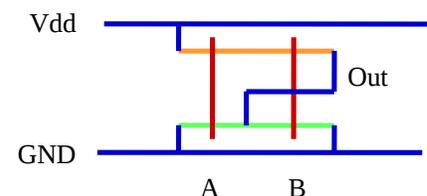
## Line of Diffusion in General



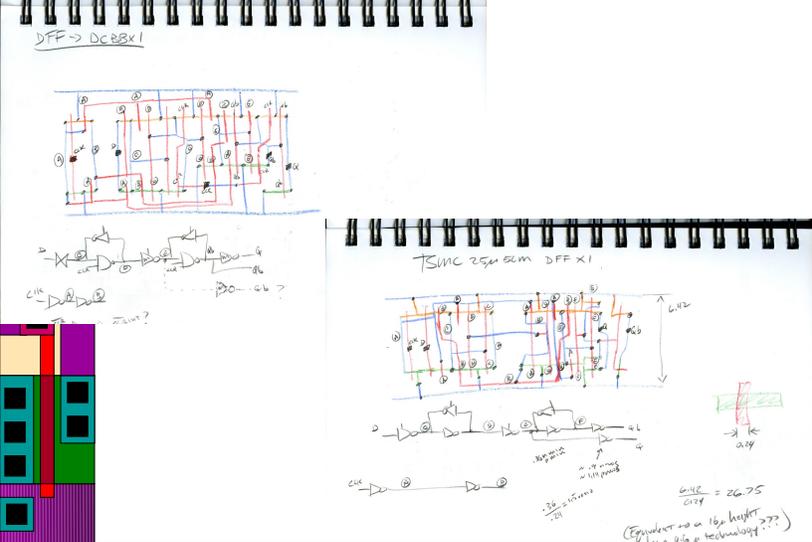
- ▶ Now break and connect diffusion
  - ▶ There's our NOR gate

## Stick Diagrams

- ▶ You can plan things with paper and pencil using Stick Diagrams
  - ▶ You'll need colored pencils
  - ▶ Draw lines for layers instead of rectangles
  - ▶ Then you can translate to layout



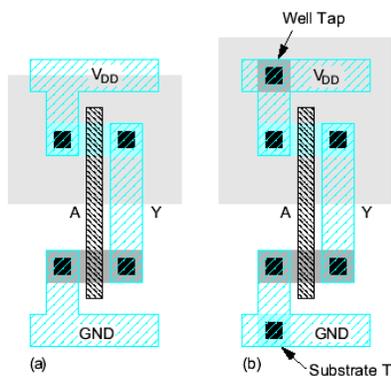
# Pre-Plan the Layout



# Gate Layout

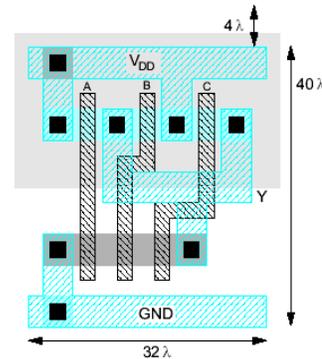
- Layout can be very time consuming
  - Design gates to fit together nicely
  - Build a library of standard cells
- Standard cell design methodology
  - $V_{DD}$  and GND should abut (standard height)
  - Adjacent gates should satisfy design rules
  - nMOS at bottom and pMOS at top
  - All gates include well and substrate contacts

# Example: Inverter



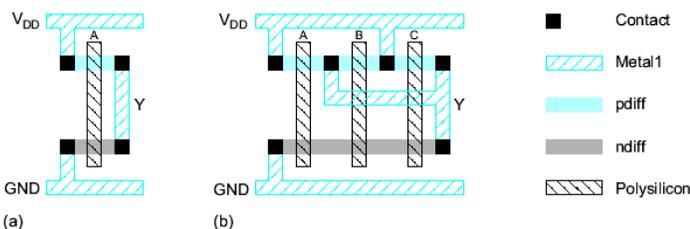
# Example: NAND3

- Horizontal N-diffusion and p-diffusion strips
- Vertical polysilicon gates
- Metal1  $V_{DD}$  rail at top
- Metal1 GND rail at bottom
- $32 \lambda$  by  $40 \lambda$
- $9.6 \mu \times 12 \mu$
- $-\lambda = .3 \mu$



# Stick Diagrams

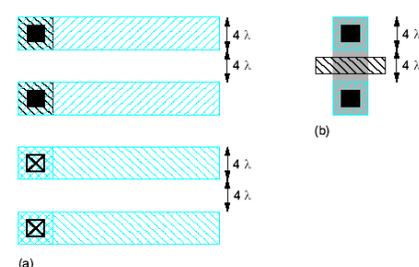
- Stick diagrams help plan layout quickly
  - Need not be to scale
  - Draw with color pencils



# Wiring Tracks

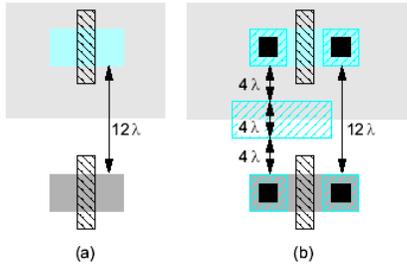
- A wiring track is the space required for a wire
  - $1.2 \mu$  width,  $1.2 \mu$  spacing from neighbor =  $2.4 \mu$  pitch
- Transistors also consume one wiring track

In our rules minimum M1 and M2 width & spacing is  $3\lambda$ , so pitch is  $1.8\mu$



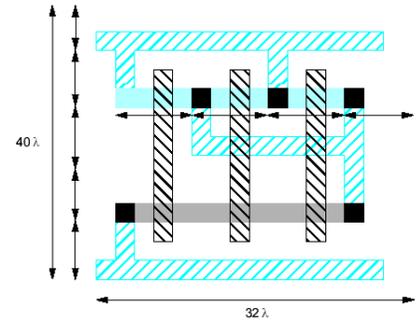
## Well spacing

- Wells must surround transistors by  $1.8u$ 
  - Implies  $3.6u$  ( $12\lambda$ ) between opposite transistor flavors
  - Leaves room for one wire track



## Area Estimation

- Estimate area by counting wiring tracks
  - Multiply by 8 to express in  $\lambda$ , or by 2.4 to express in microns



## Example: O3AI

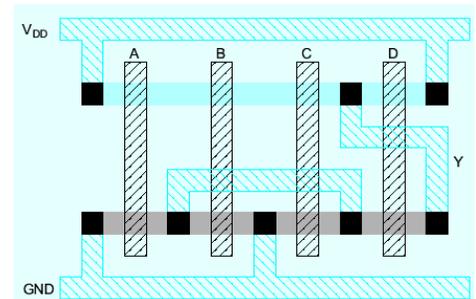
- Sketch a stick diagram for O3AI and estimate area

$$Y = \overline{(A+B+C)} \cdot D$$

## Example: O3AI

- Sketch a stick diagram for O3AI and estimate area

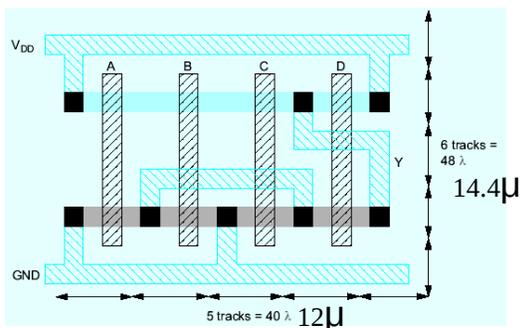
$$Y = \overline{(A+B+C)} \cdot D$$



## Example: O3AI

- Sketch a stick diagram for O3AI and estimate area

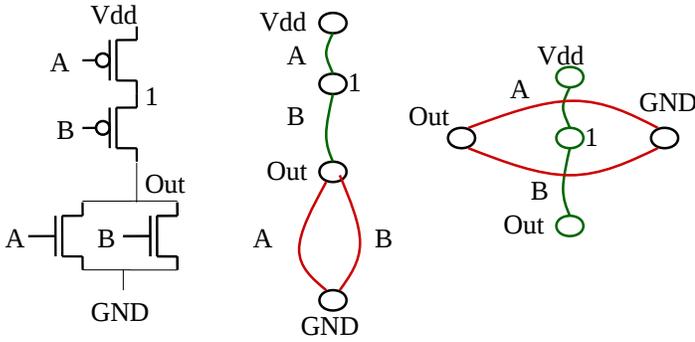
$$Y = \overline{(A+B+C)} \cdot D$$



## Euler Paths

- A graphical method for planning complex gate layout
  - Take the transistor netlist and draw it as a graph
  - Note that the pull-up and pull-down trees can be duals of each other
  - Find a path that traverses the graph with the same variable ordering for pull-up and pull-down graphs
  - This guides you to a line of diffusion layout

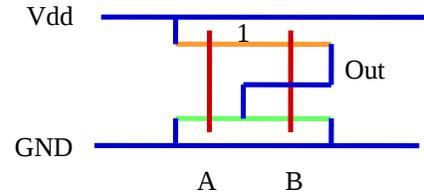
## Simple example: NOR



- ▶ Euler path is a tour of all edges
- ▶ Find a path that has the same ordering for pull-up and pull-down, i.e. **A B**
  - ▶ Vdd A 1 B Out
  - ▶ GND A Out B GND

## This Path Translates to Layout

- ▶ Find a path that has the same ordering for pull-up and pull-down, i.e. **A B**
  - ▶ You can also include all the internal nodes
  - ▶ Pull-up: **Vdd A 1 B Out**
  - ▶ Pull-Down: **GND A Out B GND**
  - ▶ Line of diffusion layout

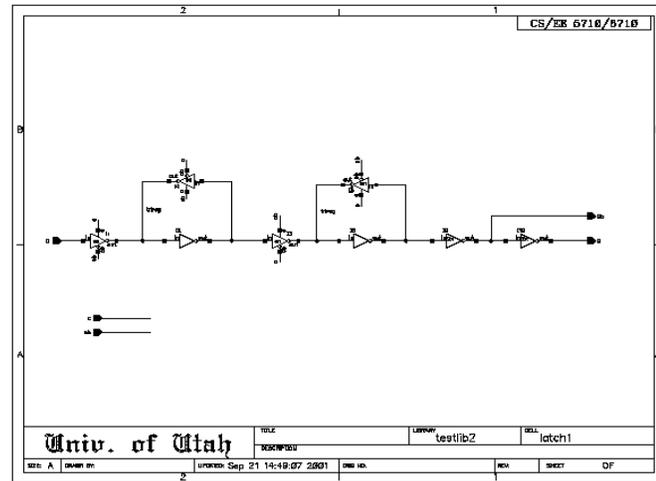


## Examples

- ▶ Switch to chalkboard for examples
  - ▶ Hopefully with colored chalk...

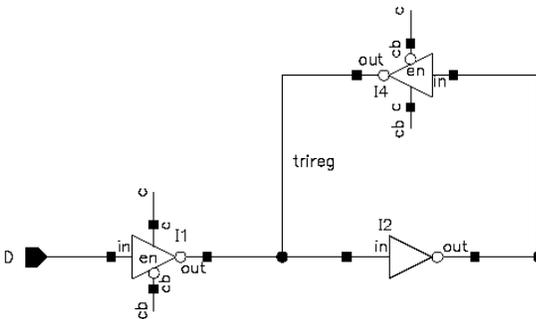
## Layout Example: Flip Flop

- ▶ Simple D-type edge triggered flip flop



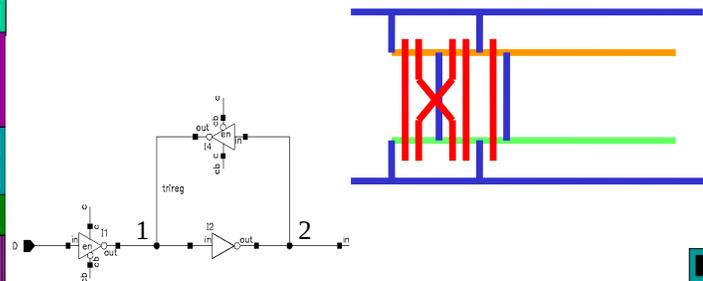
## Zoom in on Latch

- ▶ Need two copies of this for a full D flip flop



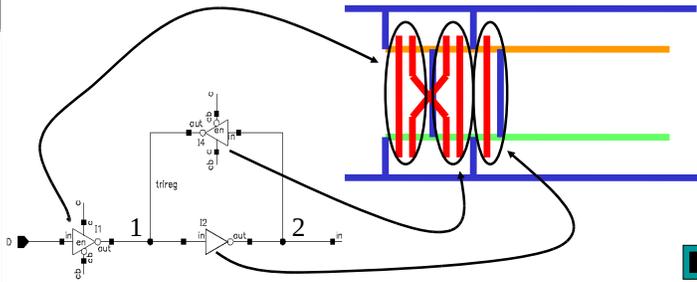
## Stick Diagram of Latch

- ▶ First add the gates
  - ▶ Note where outputs can be shared
  - ▶ Ignore details of signal crossings for now...



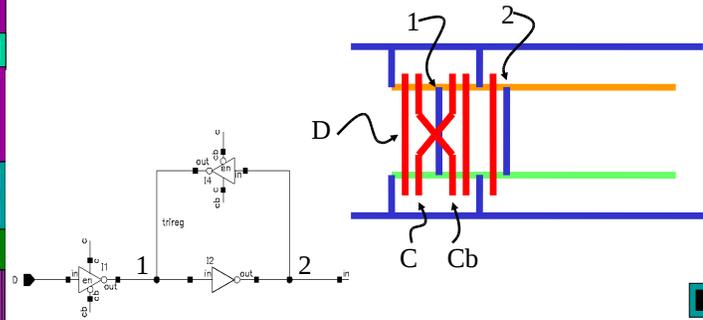
## Stick Diagram of Latch

- ▶ First add the gates
  - ▶ Note where outputs can be shared
  - ▶ Ignore details of signal crossings for now...



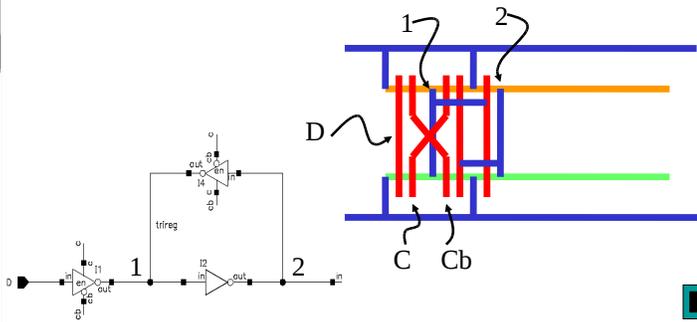
## Stick Diagram of Latch

- ▶ First add the gates
  - ▶ Note where the signals are relative to the schematic



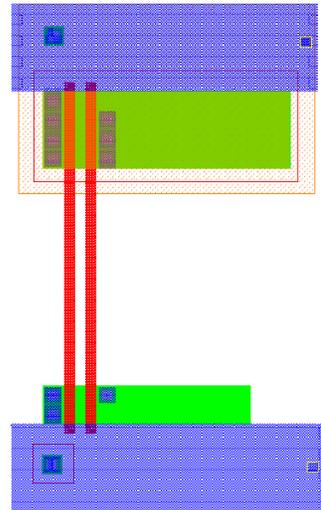
## Stick Diagram of Latch

- ▶ First add the gates
  - ▶ Note where the signals are relative to the schematic
  - ▶ Note where additional connections are needed



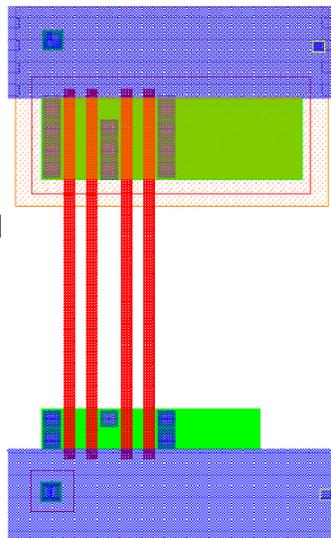
## Start With First Enabled Inv

- ▶ I'm using 5u power wires, 29u vertical pitch based on a C5x standard cell model from AMI
  - ▶ Probably overkill...
- ▶ Add DIF for N- and P-type transistors
  - ▶ Note 2x standard size because of serial connection

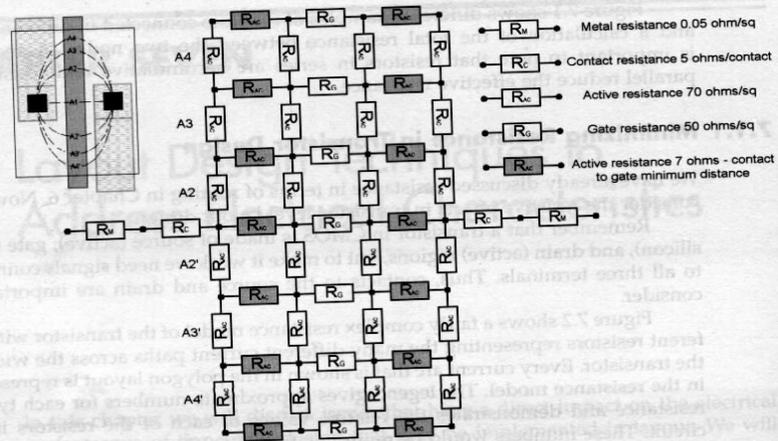


## Add Next Enabled Inverter

- ▶ Add two more poly gates for second enabled inverter
- ▶ Note that the two enabled inverters share an output (not connected yet)
- ▶ Note that I've added vdd! and gnd! For DRC
- ▶ I'll deal with C-Cb crossover later...

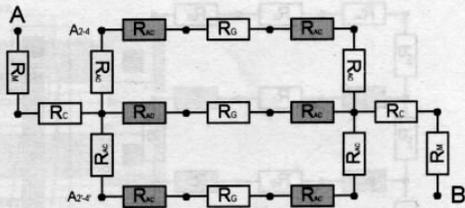
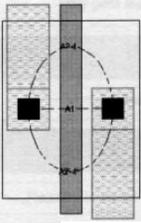


## Aside: Multiple Contacts



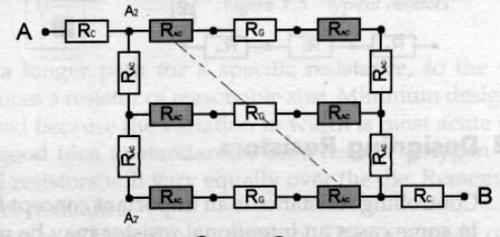
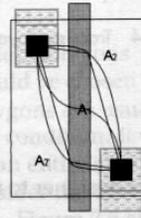
- ▶ Look at a model of transistor resistance

## Contact Option #1



- ▶ Total equivalent resistance = 56.1 Ohms
- ▶ Metal resistance = 0.05  $\Omega$ /square
- ▶ Contact resistance = 5  $\Omega$ /contact
- ▶ Active resistance = 70  $\Omega$ /square
- ▶ Gate resistance = 50  $\Omega$ /square
- ▶ Active resistance 70 - contact to gate

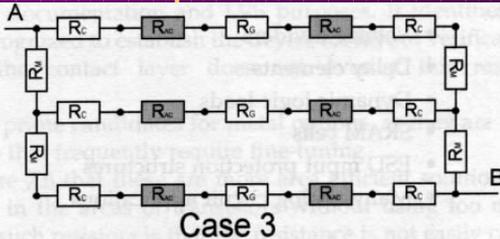
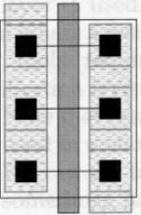
## Contact Option #2



Case 2

- ▶ Total equivalent resistance = 105.1 Ohms

## Contact Option #3

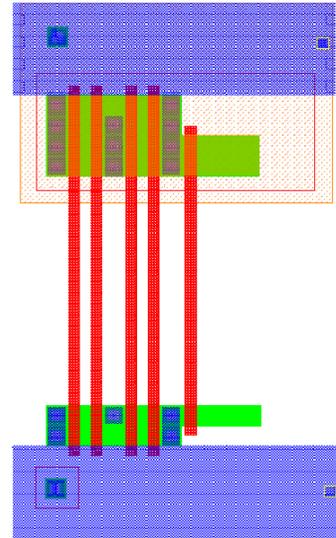


Case 3

- ▶ Total equivalent resistance = 24.7 Ohms
- ▶ So, put in as many contacts as will fit along side a wide gate...

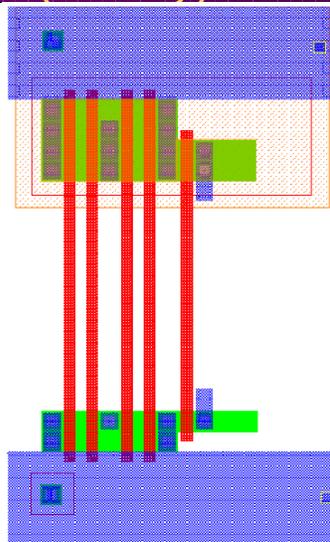
## Meanwhile, Add inverter

- ▶ Note that it's back to standard size
- ▶ Shares vdd/gnd connection with enabled inverter
- ▶ Minimum spacing for all transistors so far
- ▶ Incremental DRC at EVERY step!



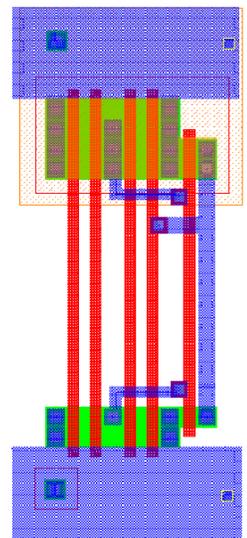
## Finish Inverter (mostly)

- ▶ Make inverter output connections
- ▶ Don't connect yet
- ▶ I'm going to use M1 as a horizontal layer
- ▶ Which means being careful about vertical use of M1



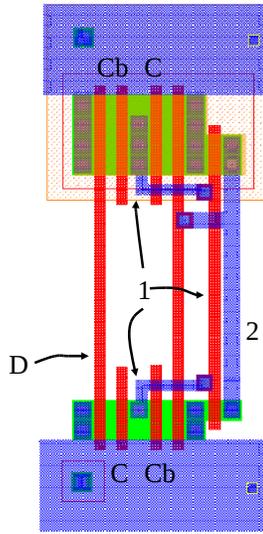
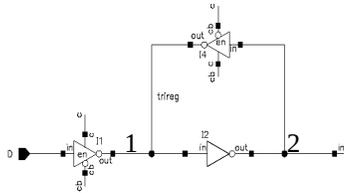
## Make Feedback Connections

- ▶ Output of inverter (connected in M1 for now) goes to input of 2<sup>nd</sup> enabled inverter
- ▶ Output of enabled inverters goes to input of inverter
- ▶ Note that output of enabled inverters goes through POLY



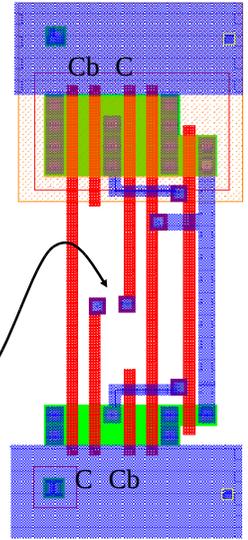
## Deal With C/Cb Crossover

- ▶ Start by cutting the “select” gates of the enabled inverters



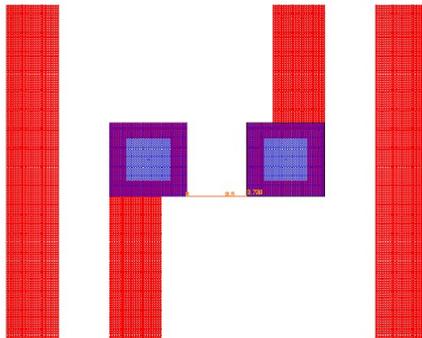
## Connect the C Input

- ▶ Prepare for M1 crossover in C wire
  - ▶ C is N-type in first enabled inverter, P-type in second enabled inverter
  - ▶ Use M1PLY contacts
- ▶ PROBLEM! We need to squeeze a poly wire inbetween those contacts...
  - ▶ Use design rules to plan for space



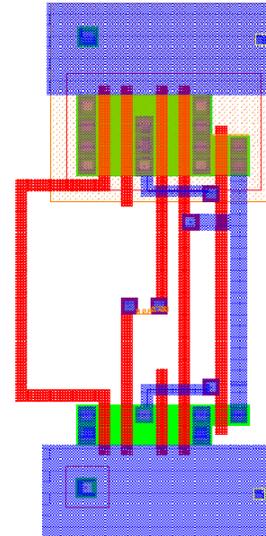
## Look at Gap

- ▶ You need to have enough space for minimum width poly to fit through gap

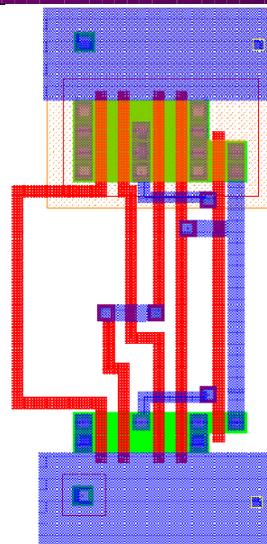


## Start Making Room

- ▶ Push D-signal poly out of the way with minimum spacing to DIF
  - ▶ We'll move it back later
- ▶ Make sure to continue to DRC at every step!

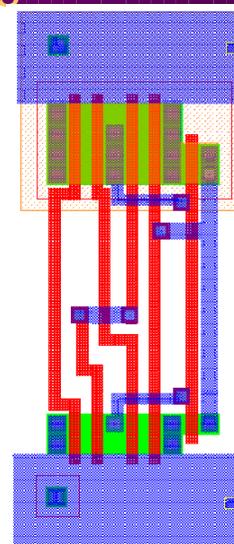


- ▶ Jog the poly around and through the gap with minimum spacing to M1PLY contact on both sides



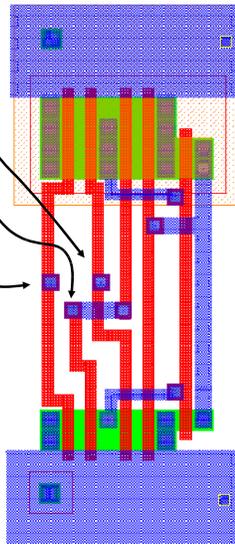
## Fit Things Back Together

- ▶ Now put big D-poly jog back as close as you can



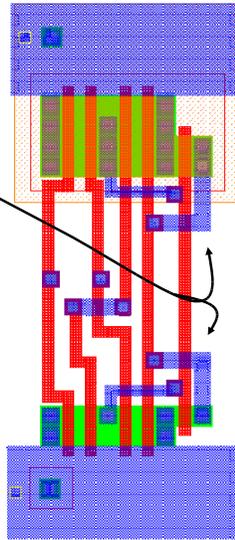
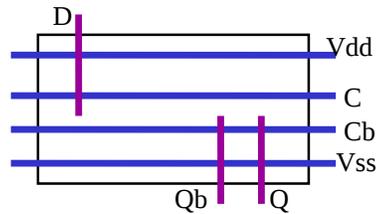
## Plan For Clock Routing

- ▶ Add M1PLY contacts for future connections
- ▶ Need to get Cb, C, D signals into the latch in the future
- ▶ Those will most likely be routed on some type of metal
- ▶ So we need the M1 metal connection at the bottom



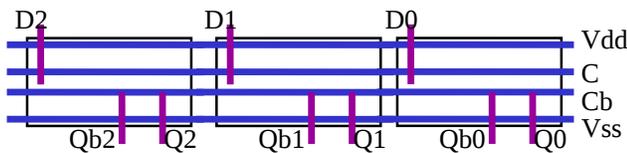
- ▶ Break M1 output connection on inverter to leave room for horizontal M1 routing

- ▶ I'll eventually route C and Cb through the cell horizontally on M1



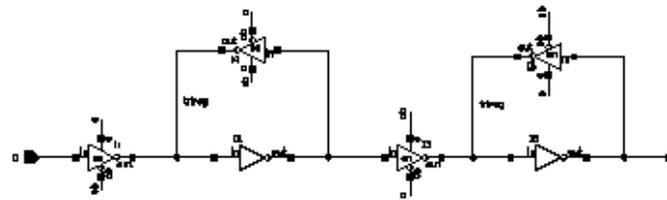
## Bit Slice Plan

- ▶ Plan is to stitch these together to make a register
- ▶ Inputs on top in M2
- ▶ Outputs on bottom in M2
- ▶ Clock and Clock-bar routed horizontally in M1



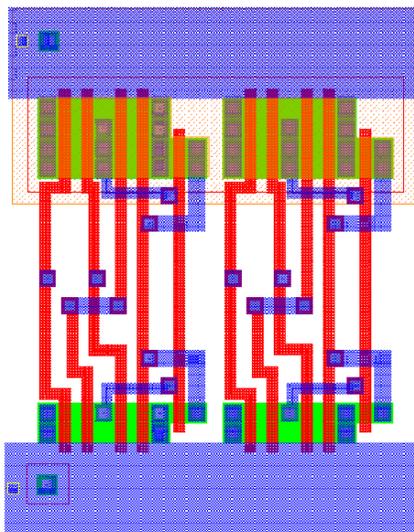
## Need Second Latch

- ▶ Basically a copy of the first latch
- ▶ But with reversed C and Cb connections
- ▶ Copy the first layout...



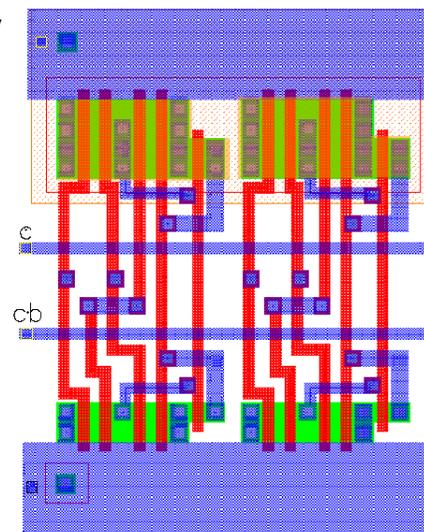
## Expand from Latch to F/F

- ▶ Select and copy the first latch
- ▶ Now I need to reverse the C and Cb connections



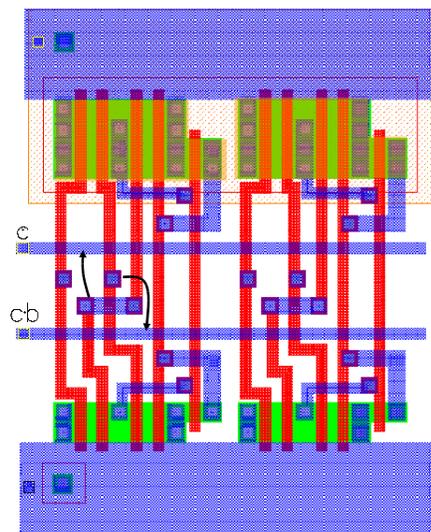
## C/Cb Routing Plan

- ▶ Remember my C/Cb routing plan
- ▶ Plan for where those wires can go



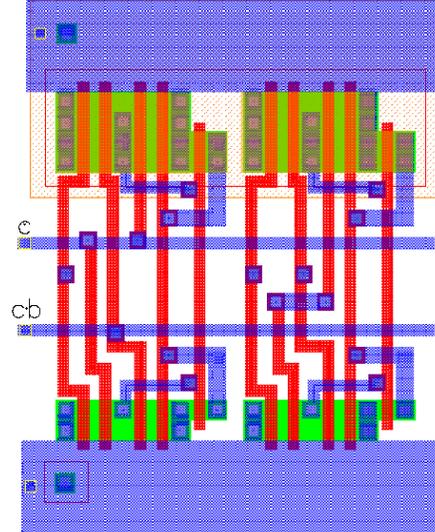
## C/Cb Routing Plan

- ▶ Remember my C/Cb routing plan
- ▶ Plan for where those wires can go



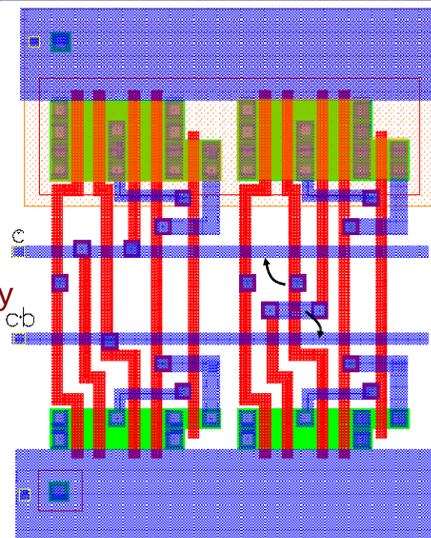
## Connect Clocks to 1<sup>st</sup> Latch

- ▶ Adjust contact positions for the first enabled inverter



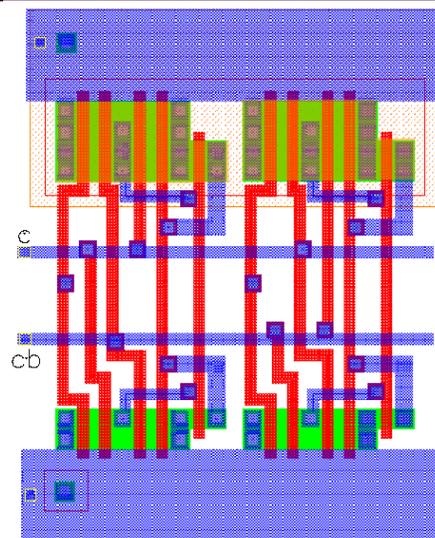
## Connect Clocks to 2<sup>nd</sup> Latch

- ▶ Now shift the contacts the other way for the second latch
- ▶ Makes the complementary C/Cb connection



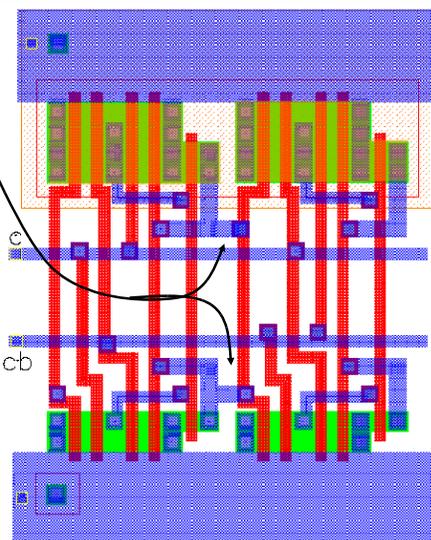
## Connect Clocks to 2<sup>nd</sup> Latch

- ▶ Now shift the contacts the other way for the second latch
- ▶ Makes the complementary C/Cb connection



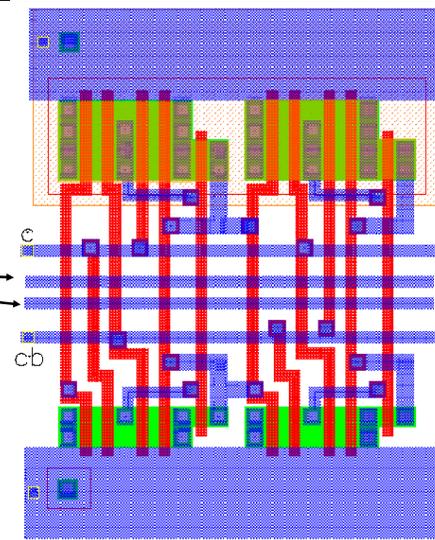
## Connect the Two Latches

- ▶ Q of first goes to D of second
- ▶ Don't really need both top and bottom connections, but it doesn't hurt
- ▶ Lower resistance paths



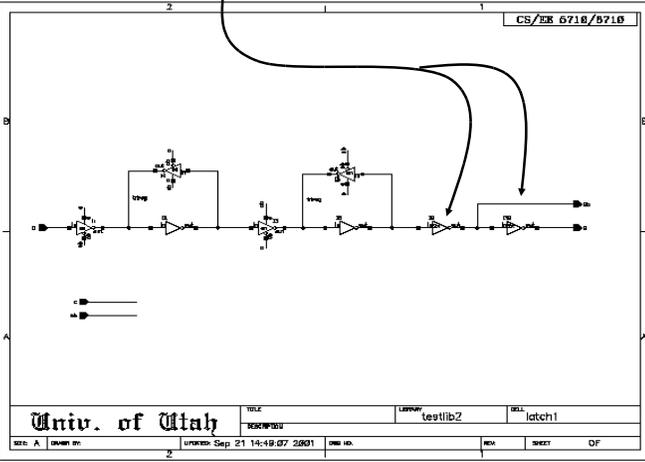
## Note Extra Routing Channels

- ▶ Note that this vertical pitch, and this cell contents have left two additional M1 horizontal routing channels through the middle of the cell



## Now Consider Output Inverters

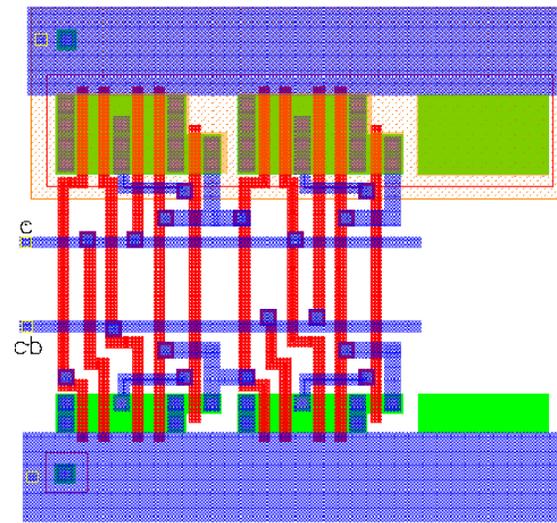
- ▶ Two more inverters
- ▶ Make them 2x size for output drive



## Output Inverters

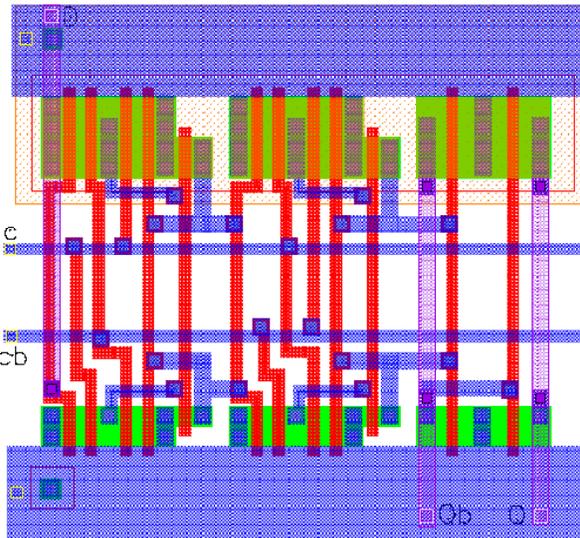
- ▶ Add the DIF for the output inverters

- ▶ Remember I want to make them 2x size



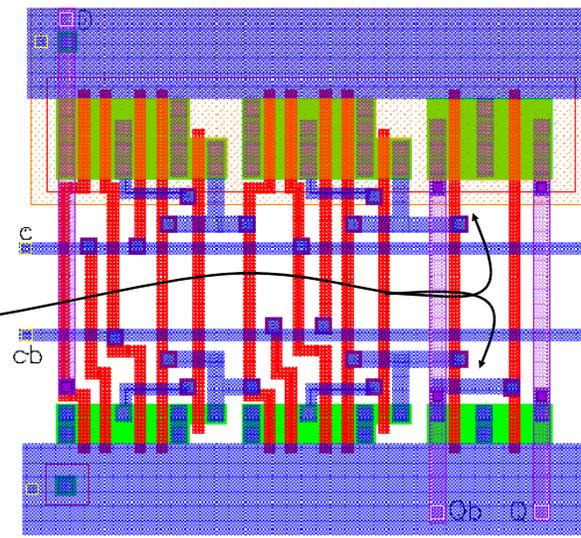
## Make Output Connections

- ▶ Add vdd, gnd and output contacts
- ▶ Add poly gates
- ▶ Make output connections in M2
- ▶ Connect to 2<sup>nd</sup> latch and to 2<sup>nd</sup> inverter



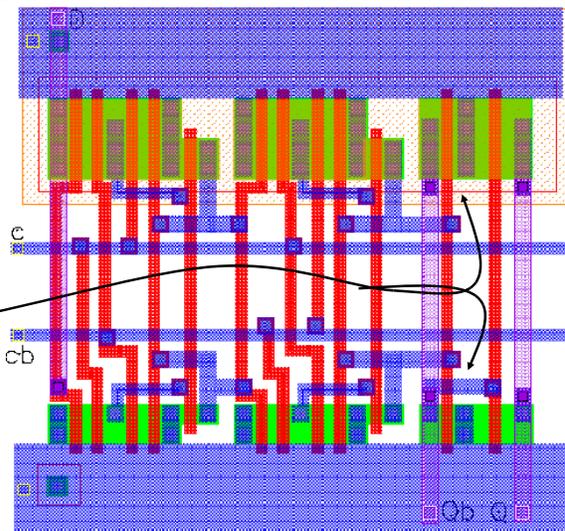
## Now Squeeze Inverter

- ▶ Select regions of the layout and stretch to move it all to a new spot



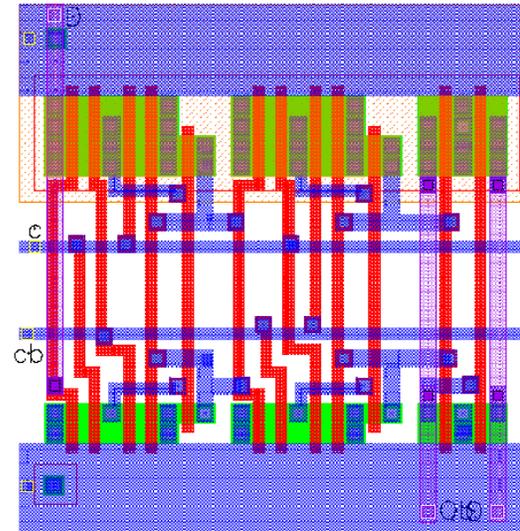
## Keep Squeezing

- ▶ Now squeeze power supply contacts



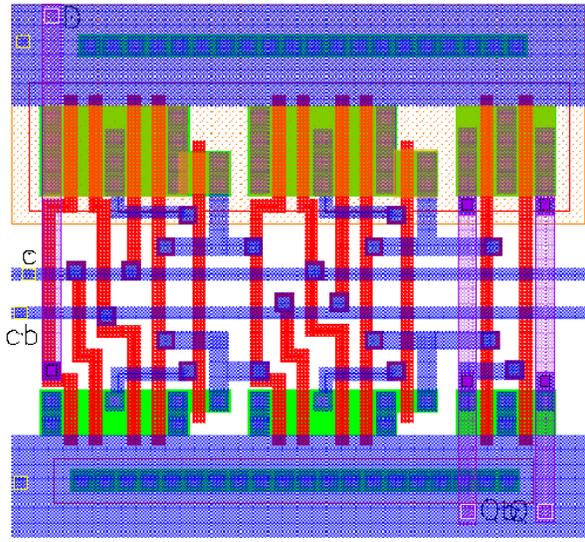
## Squeezed Version

- ▶ Output inverters squeezed together
- ▶ Note that D, Q, And Qb are routed vertically in M2

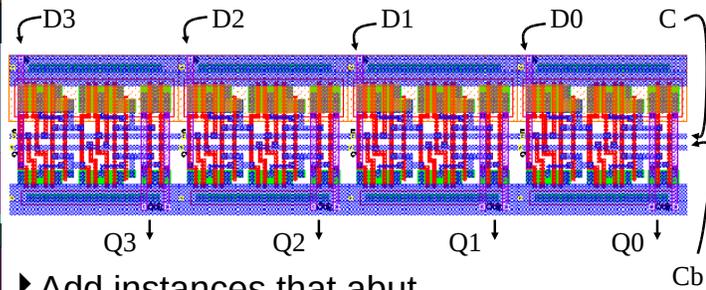


## Final D-Type Flip Flop

- ▶ Squeeze vertically since I don't need extra routing channels, and I don't need to match with standard cells
- ▶ Add long NWELL and SUB contacts

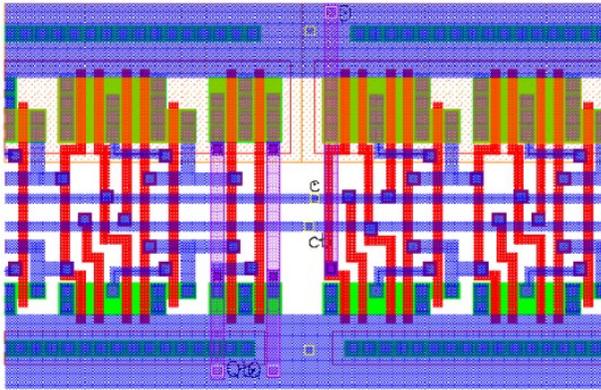


## Put Four of them Together



- ▶ Add instances that abut
  - ▶ Or use the "array" feature of the instance dialog
- ▶ Note that C and Cb are routed in horizontal M1

## Zoom in to Cell Boundary



- ▶ There's a little extra space
  - ▶ Caused by wanting each latch to DRC on its own
  - ▶ Could close this up by overlapping cells