ECE/CS 5710/6710 – Digital VLSI Design
Review of Basic Digital Design Skills
Due Tuesday September 2nd via Canvas

Instructions
This is a review quiz covering prerequisite knowledge you should have to successfully complete the Digital VLSI Design course.
Each question is worth 20 points.
This quiz is open book, and you may use and review previous course materials or other resources when taking this quiz. However, this work must be done independently without collaboration from other past or present students.
Please staple or paper clip your pages when handing them in.

Name:

1. Fundamental Electronics: (20 points)
   (a) (10 points) Consider a switch that connects a 120V source, a 23 MΩ resistor, and a 5 µF capacitor. How long should you leave the switch closed in order to charge the capacitor to 12V? Draw the circuit, set up the equation and solve for seconds.

   (b) (10 points) What is the maximum voltage that can be connected across a series combination of a 180Ω 2-watt resistor and a 120Ω 1-watt resistor without exceeding either resistor’s power rating?
2. Computer Architecture: (20 points)

Compute the following additions assuming the numbers are 2’s complement numbers. Show the result, and indicate which, if any, cause overflow.

\[
\begin{array}{ccc}
A) & 10111001 & B) & 01011101 & C) & 00100110 \\ 
& + 11010110 & + 00100001 & + 01011110 \\
& \text{----------} & \text{----------} & \text{----------} \\
D) & 01001010 & E) & 10010110 \\ 
& + 11110110 & + 01001101 \\
& \text{----------} & \text{----------} \\
\end{array}
\]

3. Finite State Machine Design: (20 points)

Design a finite state machine with one input I, and two outputs Z and E. The machine should produce a Z output whenever it has seen a 110 pattern on the input stream, except that if it ever sees a 001 pattern on the input stream, it should assert the E output, and keep that E output asserted until the machine is reset. Note that Z should never be asserted again once E is asserted. Design a state machine to implement this function. Don’t implement the circuit, just draw the state diagram for a Moore-style state machine (the outputs are determined only by the current state).
4. Circuit Timing: (20 points)

Consider the counter circuit in the following figure, which is a synchronous counter with parallel load. Assume that $T_{su}$ (setup time) is 20ps and $T_h$ (hold time) is 5ps for the flip flops. Assume that $T_{pd}$ (propagation delay) through each gate (AND, XOR, and MUX) is 30ps.

What is the maximum clock frequency for which the counter will operate correctly? Why?
5. Combinational Logic: (20 points)

Convert the following circuit to an equivalent circuit that uses only NAND gates with non-inverting inputs. Do NOT minimize or optimize the circuit, just change the gate types. (Hint: apply deMorgan’s theorem $\overline{A \land B} = \overline{A} \lor \overline{B}$.)

![Circuit Diagram]