Variation in our Designs

Ken Stevens
Variation

The electrical behavior of our chips are impacted by two main sources of variation:

1. Environmental factors
   - These arise based on ambient and operational conditions of a circuit:
     - voltage, temperature fluctuations

2. Physical factors
   - Due to non-ideal patterning and implantation in physical circuit
     - process variation
   - a.k.a. parametric variation
Variation

The big three for variation in an integrated circuit are:

- **PVT**: Process, voltage, temperature
  - Coupling *could* be argued as a voltage variation, but is normally considered independently.
Variation

There are significant differences between Environmental and Physical variation:

- **Process variation**
  - Static once the chip has been fabricated
  - Usually follows a normal distribution
  - Correlations are usually related to physical distance

- **Environmental variation**
  - Variations can change dramatically on a circuit based on operating conditions
  - Statistical distributions may or may not apply
  - Correlations may be physical or operation dependent
Classification

- Electrical behavior
  - $L_e$
  - $V_{th}$
  - Width
  - Interconnect

- Spatial behavior
  - wafer to wafer
  - die to die
  - within die

$(CD = \text{Critical Dimension})$

$L_e = \text{effective channel length}$

Nagib Hakim, Intel
Classification

- Systematic
  - Smooth, distant dependent
  - Known change with distance
  - CD, COV, Metal R & C, $V_{dd}$, Temp

- Random
  - “White” noise
  - Distance independence
  - $V_{th}$

(COV = OVerlap Capacitance)

Samie Samaan, Intel
Sources of Variation

- Photolithography
- Gate etch
- Ion implantation
- Thermal processing
- Mask alignment
- Feature angles
- Temperature
- Polishing
- Photoresist molecule size
Significant increase in variations of effective channel length $L_{eff}$, wire parameters dimensions and resistivity ($W,T,H,\rho$), and transistor parameters such as oxide thickness and thresholds ($T_{ox}, V_t$).
Process Variation Scaling

There is significant controversy over process variation scaling

- Common claim of loosing a full technology generation due to variation
- Many means of reducing variation at various costs
- Some factors truly are random effects
  - number of dopant atoms
Process Variation Scaling

- Some companies play both games
  - “We must find solutions or variation will significantly damage us.”
  - “We know how to mitigate variation so it won’t impact us much.”

- Even process aware design loses 15% performance to process variation

- All agree solutions must be found and design will be impacted in some form
  - Statistical CAD
  - Design constraints
  - Increased $W$
Variability Classes

What is difference between *variability* and *uncertainty*?

- Uncertainty: sources unknown or model too difficult or costly

Lack of modeling turns variability into uncertainty...

Classes of Variability

<table>
<thead>
<tr>
<th>Class</th>
<th>Time Scale</th>
</tr>
</thead>
<tbody>
<tr>
<td>Physical</td>
<td>$10^6$</td>
</tr>
<tr>
<td>Environmental</td>
<td>$10^{-4}$ to $10^{-6}$</td>
</tr>
<tr>
<td>Functional</td>
<td>$10^{-12}$</td>
</tr>
</tbody>
</table>
## Lithography Issues

<table>
<thead>
<tr>
<th>Wavelength</th>
<th>Year</th>
</tr>
</thead>
<tbody>
<tr>
<td>365nm</td>
<td>to 1992</td>
</tr>
<tr>
<td>248nm</td>
<td>to 2000</td>
</tr>
<tr>
<td>193nm</td>
<td>current</td>
</tr>
</tbody>
</table>

1. 193nm light etching $< 14$ nm features
2. Major pattern sensitivity to neighborhood
3. Poly line edge roughness of $80\text{Å} \approx 25\%$ length variation
Lithography Issues

(Source: Shekhar Borkar)
Lithography Issues

- Semiconductor manufacturing requires best lenses and data rates in the world.
  - 1mm slit 22mm long scan 36 mm in < 1 second
  - $2 \times 10^{10}$ feature pixels with 1/30 feature accuracy
  - Data transfer rate 20 TeraHz (not possible maskless)
- Tool cost sharing part of Moore’s Law
Lithography Issues
Scaling and Technology Requirements in Wavelengths and \( \mu/\text{NA} \)

<table>
<thead>
<tr>
<th>CD (nm)</th>
<th>45</th>
<th>32</th>
<th>22</th>
<th>16</th>
<th>11</th>
<th>7</th>
</tr>
</thead>
<tbody>
<tr>
<td>CD/193nm</td>
<td>1/4</td>
<td>1/6</td>
<td>1/9</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CD/(193nm/1.46) Immersion 132nm {\text{NA}_{\text{EFF}} = 1.35}</td>
<td>1/3</td>
<td>1/4</td>
<td>1/6</td>
<td>1/8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(n_{\text{FLUID}}) 1.55 to 1.75</td>
<td>1/3</td>
<td>1/5</td>
<td>1/7</td>
<td>1/10</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CD/(13.3nm/0.3) EUV NA = 0.3</td>
<td>1/2</td>
<td>1/3</td>
<td>1/4</td>
<td>1/6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CD/(13.3nm/0.5) EUV NA = 0.3</td>
<td>0.6</td>
<td>0.4</td>
<td>1/4</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Single Exposure, Double Patterning, \( \text{N}>2 \), Impossible**
The above values are roughly normalized \( k1 = \frac{\text{CD}}{\lambda/\text{NA}} \)

Andy Neureuther
Lithography Issues

Double Patterning
A method to break the 0.25\(k_1\) barrier

Double patterning:
a method to break the 0.25 \(k_1\) barrier

Issues are alignment and tech profile.
Lithography Issues

Pitch Division by Spacer Technology

- Deposition and etch back doubles number of lines
- Control is non-lithographic process
  - Issues are duty cycle and spacer shape
Reaching 7nm Summary

- Five generations are technically feasible beyond the 45nm generation.
  - Extend current technology by double patterning, pitch division, alignment, new processes and materials.
  - Extreme Ultra Violet (EUV) could compete at 22nm with triple/double patterning if ready in 2013.
  - Issues are source power, resist resolution, roughness, and cost.
- 7nm technology might reach production in 2020.

However technically feasible, it is questionable if they are economically feasible and will provide reduction in cost per logic function.
Lithography Issues

1. Random dopant fluctuation
   - Only a few hundred dopants in channel
   - $200\text{mV} V_t$ shifts & $100 \times$ leakage
   - 1MBit SRAM yield requires redundant cells:
     - 90nm: 3, 65nm: 230, 45nm: 10K

2. Oxide scaling: major power issue
   - 11Å is approx. 6 atomic layers
   - Visualize a film 6 atomic layers thick covering area of $10^9$ atomic layers wide on 300mm wafer

3. Negative Bias Temperature Instability: NBTI
   - At negative bias and elevated temp, pFET $V_t$ shifts more negative
Back End Issues

- Chemical Mechanical Polishing – **CMP**
  - Dishing
  - Optical resolution on subsequent higher layers
- Variation in capacitance on wires: 50%
- Workload variability of 5% to 95%: power, cooling, performance
- On-chip supplies: 15% supply droops
- Thermal: ambient and self-heating
CMP and Metal Density

Mechanical planarization of deposited material

Low M2 Pattern Density
Decreased ILD Loss

High M2 Pattern Density
Increased ILD Loss

Bernie Landau, Intel
CMP and Metal Density

Mechanical planarization of deposited material

“Dishing” affects wider metal lines
  - metal line cross-section is not rectangular

What is the maximum metal width rule in 500nm process?
What is it for a 65nm design?
CMP and Metal Density

Mechanical planarization of deposited material

“Dishing” affects wider metal lines
-metal line cross-section is not rectangular

What is the maximum metal width rule in 500nm process? None!
What is it for a 65nm design? 12µm!
Source of Parametric Variation

- Lithography
  - optics
  - wavelength
  - planarization
  - reflections
  - pattern dependencies

- Doping

- Defects
  - crystal impurities
  - dust

- Mechanical
  - stepper motors and accuracy
Statistical Models

Statistical descriptions of parametric variation

1. Estimate characteristics or statistical distributions
2. Understand or minimize impact on performance
Lumped Statistics

Basic approach:

- Characterize distribution over sample set
- Estimate statistical moments to create distribution
- Empirical method: physical sources not considered
- Deterministic (not understood) and random contributions lumped into statistical description

Example:
- Measure channel length of fixed design size across wafer
- Find normal distribution
- Estimate mean and standard deviation $\sigma$
Lumped Statistics

Basic system approach

- Assume all variation is random
  - Some variations are **systematic** and predictable
- Treat each variable as independent
  - Some parameters are correlated
- Determine the margin required for yield
  - Typically $3\sigma$ for speed paths, $4-5\sigma$ for races
Parametric Variation Classes

For design purposes, there are two important classes:

1. Inter-die variation
2. Intra-die variation

Our current 300mm (12 inch) wafers contain thousands of die (chips)
**Inter-Die Variation**

- Parametric variation inside a nominally identical die
- Shift in the mean of some parametric value across all devices on a chip (die)
- Also called *die-to-die variation*
- Normally assume different physical source: independent variables
- Variation mainly due to
  - steppers and non-planarity
- Solution:
  - process corner simulation
  - fast or slow skewed transistors, chips, etc.
Intra-Die Variation

- Deviations occurring within a single die (chip)
  - Loss of matched behavior between structures
- Also called *within-die variation*
- Variations due to:
  - Random dopant fluctuations, planarization, reflections, pattern dependencies
- Solutions:
  - Design constraints
  - Worst-case modeling
  - Statistical timing analysis
Inter- and Intra-die Variation
Mechanisms of Process Variation

Device Geometric Variation

- Affects transistors, resistors, capacitors, etc.
- Channel length $L_{\text{eff}}$, gate oxide thickness, width
  - $L_{\text{eff}}$ most significant
Mechanisms of Process Variation

Device Geometric Variation (cont.)

- A lithographic source
  1. Film thickness variation
     - gate oxide thickness
     - relatively well controlled
     - usually a die-to-die issue
  2. Lateral dimension variations
     - photolithographic proximity effects
     - *systematic* pattern dependencies
     - mask, lens, or optics deviations
     - plasma etch dependencies
Mechanisms of Process Variation

Device Material Parameter Variation

1. Doping fluctuations
   - Due to dose amount, energy, angle variation, or thermal annealing
   - Truly random distribution
   - Affects junction depth and dopant profiles, electric parameters like threshold
   - Exacerbated by drain engineering (retrograde doping: halo)

2. Deposition and anneal
   - Due to deposition variation, silicide formation, grain structure

Affects contact and line resistance
Mechanisms of Process Variation

Device Electrical Parameter Variation

1. Threshold and leakage
   - Random placement and concentration of dopants
   - Significant affect at 100nm and smaller
   - In 25nm node $V_t$ uncertainty $\sim \frac{10}{\sqrt{W}}$ mV per $\mu$
   - Most affects small devices and those that must be well matched (RAM blocks)

Note energy / variation tradeoff!
Mechanisms of Process Variation

Interconnect Geometry Variations

1. Line width and spacing
   - Due to photolithography and etch dependencies

2. Metal thickness
   - Sputter etched or deposited films
   - Dishing and erosion in damascene (copper polishing) processes

3. Dielectric thicknesses
   - Chemical mechanical planarization: CMP
   - Deposition of high density plasma (HDP)
Mechanisms of Process Variation

Interconnect Geometry Variations (cont.)

1. Contact and via size
   - Etch depth results in different degrees of lateral openings, resistance
   - Etch process variation
   - Systematic layer dependencies

These all have a significant systematic pattern dependence 10-20% variation in damascene, 5% for deposition.
Mechanisms of Process Variation

Interconnect Material Parameter Variations

1. Contact and via resistance

2. Metal resistivity and dielectric constants
   - Large wafer-to-wafer variation

Pattern dependencies and directional effects might be important for low-$\kappa$ dielectrics
Characterizing Process Variation

Statistical modeling and optimization for process variation

1. Extraction of statistical device models
2. Sensitivity analysis to estimate the magnitude
3. Worst case methods for design guard-bands
4. Spatial modeling and mismatch analysis
Statistical Device Model Extraction

Spice Level 1 MOSFET model for saturation current:

\[ I_{ds} = \mu C_{ox} \frac{W}{L-\Delta L} (V_{gs} - V_{th})^2 \quad \text{for} \quad 0 < V_{gs} - V_{th} < V_{ds} \]

- Many quantities not directly measurable (e.g. \(\Delta L\))
- Infer parameters using **Model Parameter Extraction**
  - Infer from measurement of \(I_{ds}\) versus \(V_{gs}\) and \(V_{ds}\)
  - Approximation with finite tolerances
  - Subject to error
- Perform extraction on large population of parameters \(P\)
- Estimate statistics of \(P\)
Sensitivity Analysis

Relate electrical/simulation results to $P$ such as geometric variation

- Monte Carlo methods

- Use function $f$ to propagate $P$ to $Q$: $Q = f(P)$
  - Use 1$^{\text{st}}$ order expansion of analytical function $f$:
    
    $Q + \Delta Q = f(P + \Delta P)$
    $\Delta Q \approx \left\| \frac{df}{dP} \right\| \Delta P$
    
    - $\Delta P$ and $\Delta Q$ are usually standard deviations
    
    - Assume normal distributions, allows variance to propagate as:
      
      $\sigma^2_Q \approx \left( \frac{df}{dP} \right)^2 \sigma^2_P$
Worst Case Analysis

Most common mechanism for analyzing variation is worst-casing. However, various components of $P$ can be correlated.

- Ignoring correlation gives extreme over-pessimism.
Worst Case Analysis

- Goal: measure quality or *yield* of design
  - Yield: percent of circuits that meet specification

- Computing yield directly expensive
  - \( f \) typically requires complex circuit simulations and statistical evaluation: \( z = f(P) \)
  - Example: \( z \) is performance, \( P_{wc} \) are process corners . . .

- Worst-case models are indirect method of bounding yield

- Normally give unique settings for worst case parameters for each yield value for similar structures (e.g. cell library)
  - delay, power dissipation, noise immunity, leakage, . . .
Spatial Variation Modeling and Mismatch

Device matching is moving from analog to digital domain

- When $\Delta P > 0$, we have mismatch or variance
- For truly independent variables, worst mismatch $\approx 2\Delta P$
- Many interesting dependencies can exist:
  - Area
    - Larger areas average variations, reduce $\Delta P$
    - Tradeoff mismatch for larger sizes
  - Physical (spatial) separation
    - Larger systematic or die-to-die variation when in proximity
    - Good model: mismatch $\sim$ square of distance
  - Other spatial systematic parameters
Systemic Spatial Issues

Many spatial (layout) parameters effect variation

- If $P$ has spatially systematic component:
  \[ P = P_0 + \mathcal{F}(x, y, \theta) + \tilde{P}_\varepsilon \]
  where $P_0$ is the die mean, $\mathcal{F}$ is spatial distribution, $\theta$ random component, $\tilde{P}_\varepsilon$ remaining random variation

- Without layout information, analysis uses full random distribution

- Locality information $(x, y)$ bounds variation to fully apply systematic to fully random distribution based on proximity
Optical Proximity Correction

**OPC** is an up-front compensation for diffraction and interference as a result of a photo-mask

- These are systematic variations
- Compensate for errors due to
  - Diffraction, process effects, line width difference
  - Edge vs center of arrays
  - Nested vs isolated lines
  - Line end shortening
- Sometimes thousands of polygons in a single gate transistor
- Exponential increase in mask data size
Physical Variation Reduction Process

A plethora of techniques used to reduce variation

Andy Neureuther, UCB
Source-mask optimization at work for low k1 imaging
65 nm DRAM brick wall, 0.93 NM, 193 nm dry, $k_1 = 0.31$

No OPC  Rule based OPC  Model-based OPC  Mask

Optimized  Optimized  Polarized  Source

Process window [nJ/m]

Andy Neureuther, UCB
Clock Tree Example

- All systematic parameters set to zero
- Metric $z$ is amount of skew between two leaves in H-Tree
- Three sources of variation:
  - Random channel length $L_e$ variation $\Delta L$
  - Random wire width variation $\Delta W$
  - Proximity variation in $L_e$
Clock Tree Example

Parameter extraction for 250nm process node:

- Random channel length $\Delta L$
  - 65 samples on central buffers and loads
  - $N(0.0, 35\text{nm})$ tolerances

- Random wire width $\Delta W$
  - 63 samples, one in each segment of H-Tree
  - $N(0.0, 250\text{nm})$

- Spatial channel length $\Delta L$
  - Uniform distribution assumed
Clock Tree Example
Random Channel Length (a), Random Wire width (b), and spatial channel length variation (c) of H-Tree design
Clock Tree Example

Results at $3\sigma$

- Random $\Delta L$
  - constrained 139ps vs. worst case 172ps
- Random $\Delta W$
  - constrained 41ps vs. worst case 49ps
- Spatial $\Delta L$
  - 10ps
H-Tree Statistical Interconnect Impact

Studies using wire width with ILD thickness variation of 3%

- Statistical nature of wires
  - Variance $\sigma_L^2$ in parameter $P$ of interconnect
  - Broken up into $n$ segments of length $L_i$
  - Total variance $\sigma_P^2$ reduced to $\sigma_P^2 = \frac{\sigma_L^2}{n}$

- In hierarchical wire design (wider trunks)
  - Delay variation is $\sim 48\%$ of total delay
  - Wire delay only 12\% of that variation

- In data path structures with short wires
  - Variation $\sim 18\%$ of total delay
  - Device delay is 48\% and wire delay 52\% of variation
Interconnect Studies

pattern dependent ILD variation in top level metal in 1GHz design (pg 112)

Affect of fill on pattern dependent wire variations
Main MOSFET Variations

Primary MOSFET variations

- Effective Channel Length
- Poly CD
- Threshold
- Overlap capacitance

$L_e$ and $V_t$ are largest and most important
Scaling

Increasing variations

- $V_t$ and $L_e$
  - Mainly due to random dopant fluctuations ($V_t$) and photoresist molecule size and placement ($L_e$).

Slightly decreasing variations

- Wire variations
Major Problem Categories of Variation

1. Resiliency
   - No longer *defect* related, but now *degraded*
   - Example: Good contact was $1 \Omega$ vs $1 \text{M}\Omega$.
     Values spreading, “good” contact ranges from $1 – 100\Omega$.
   - This spreads into “bad” value ranges and becomes aging risk

2. Scalability
   - 50 design rules for Mead/Conway vs 300 in 90nm
   - Rule creep initially for defects and yield: e.g. aligned transistors
   - Process shrink/migrateable designs a dream?
   - Physical abstraction broken - e.g. antenna problem
Major Problem Categories of Variation

3. Lithographic Abstraction and Composability
   - Behavior depends on neighborhood
   - ...Now beyond cells ... Not just placing "bricks"
   - OPC modifications enormous!

4. Functional Abstraction
   - off currents equal to on currents
   - no longer holds: tout = tin + delay(slope, load)
   - Can’t treat transistors as simple logic or booleans (on or off)
   - other second order phenomenon
Coping

1. Know Thine Enemy: Can’t fix what you can’t measure
   - On-chip monitors of thermal, performance Ring Oscillator’s, supply, aging...
   - IBM Data: 12 ring oscillators on die, about 200% variation for single oscillator (total die-to-die) and a 50% variation within die.
   - At-speed scan testing

Get data to understand models, use data to drive our CAD models. Raise level of abstraction of cell to placement aware and interconnect aware.
Coping

2. Statistical Static Timing Analysis (SST)
   - Constant + sensitivities + global variation + random
   - Path based SST
   - Can’t do corner-based modeling anymore

3. Adapt with Design approaches
Adaptations

1. Multiple supply voltages
2. Body Biasing
3. Dynamic Voltage and Frequency Scaling
4. Throttling
5. Efficiency scheduling
6. Multi-Cores
Process and Design Adaptations

7. Metal patterning insertion

8. OPC

9. Poly (transistor) alignment

10. Spatiality

11. Pattern dependencies and reflections
    - densities, hammer-head to avoid finger reduction, ...
Design Approaches

12. Averaging effects
   - Increase sizes
   - Long paths
   - Shorting outputs
   - Legging?

Our future high performance designs:
   - Sea of Gates
   - FPGA like design
One More Issue

Power is a big issue, so we want to lower $V_{dd}$ if possible, right?
Maybe...

For ultra-low power design, variations dramatically increase below $V_{th}$ exacerbating exponential drop in performance.
Review

1. two main sources of variation (environmental, physical)
2. PVT
3. amount of process variation delay
4. sources of parametric verification
5. systematic vs. random variations
6. how generate statistical models
7. why use statistical models
8. typical margins in $\sigma$ for speed paths and races
9. die-to-die variation, cause
Review

1. best die-to-die model
2. within-die variation, cause
3. evaluation models
4. variation topology of two main die variations
5. geometric variations, source
6. material parameter variations, causes and affects
7. electrical parameter variation
8. CMP
9. statistical characterization
Review

1. model parameter extraction
2. sensitivity analysis
3. worst case models
4. yield
5. spatial variation, systematic issues
6. OPC
7. most important MOSFET variations
8. design means of reducing variation
9. future design appearance to mitigate variation