

**ECE 6770 FINAL PROJECT**

**POINT TO POINT COMMUNICATION SYSTEM**

**Submitted By:**

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## MOTIVATION

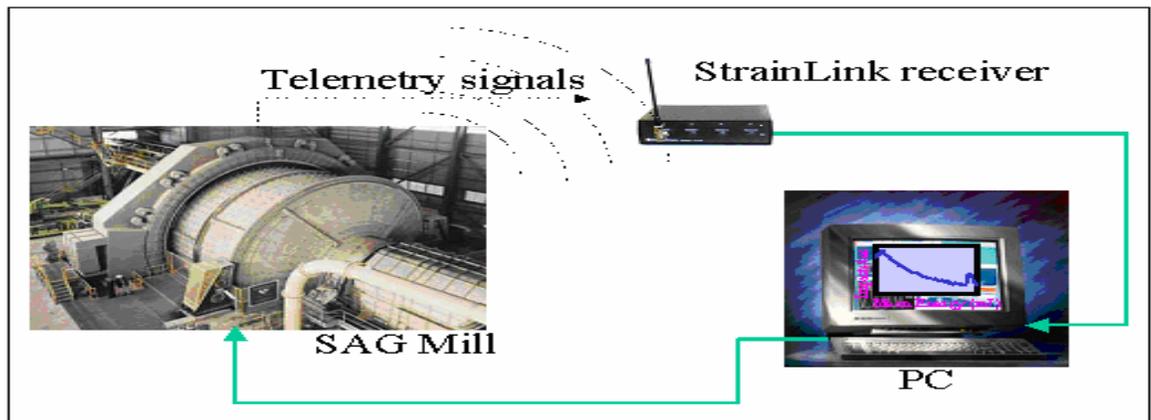
Often in the real world we have situations where remote monitoring is very essential as it is near impossible to have a look at operations as and when they happen. The mining industry is an example. There are huge crushing and grinding mills where large rocks are broken using 5 inch diameter balls. Now in such a setup it is very difficult to have wires running from sensors to the system or have data loggers as the system will not shutdown for months. Hence the only viable option is to have a wireless system.

The basic aim of our project is to implement a point to point communication link which can transmit data at high rates.

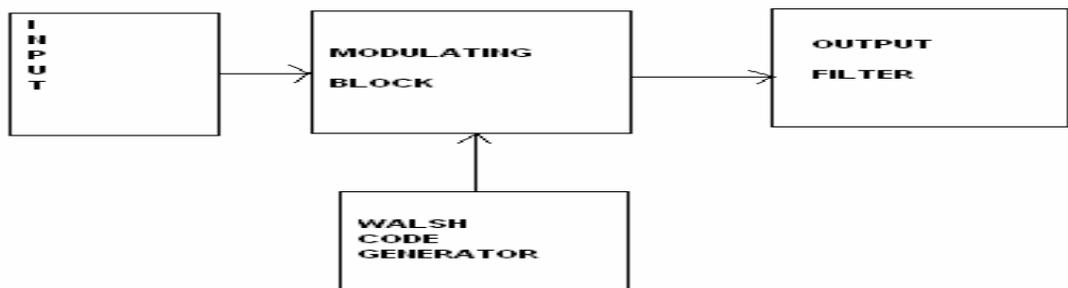
## INTRODUCTION

The system that we implemented is for a mining company.

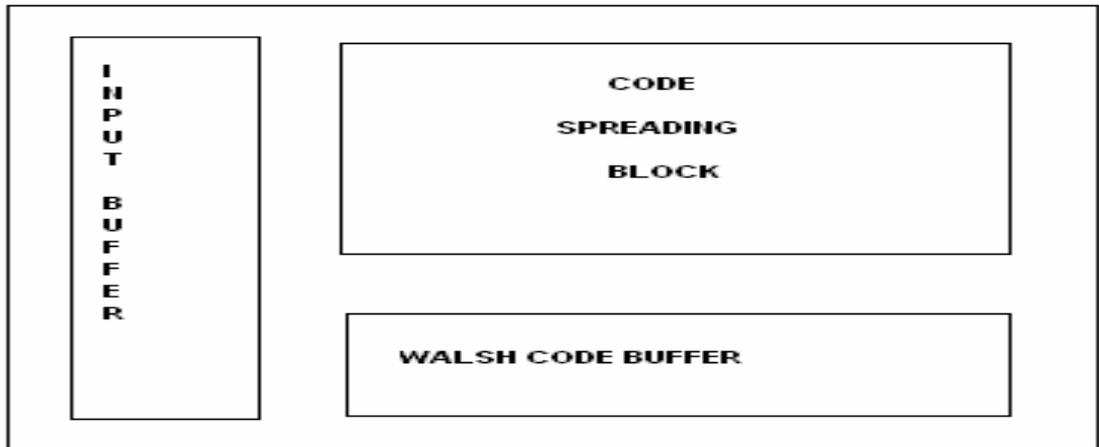
Communication in grinding mills is inherently inefficient using only About 1 percent of the energy. Any monitoring of the feed can increase the efficiency by about 10%.The data from the sensor inside is transmitted at 100,000 samples/second. An external receiver will collect the data and this data would be analyzed real time by a machine.



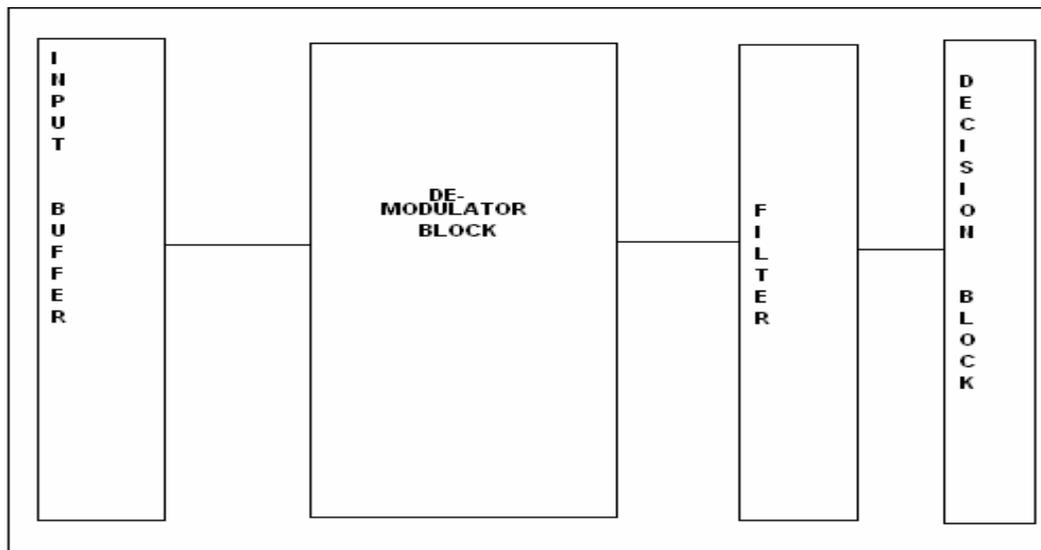
The overall schematic of the transmitter is shown below .



The above block diagram shows 4 important blocks. The input section is where the ADC is present. The modulating block is CDMA. CDMA does not assign a specific frequency to each user. Instead, every channel uses the full available spectrum. Individual conversations are encoded with a pseudo-random digital sequence.



The above diagram shows the Modulating section, which is made by using digital libraries. The code generator is specific for the chip and is hard-coded in the chip. This is what acts as the device signature.



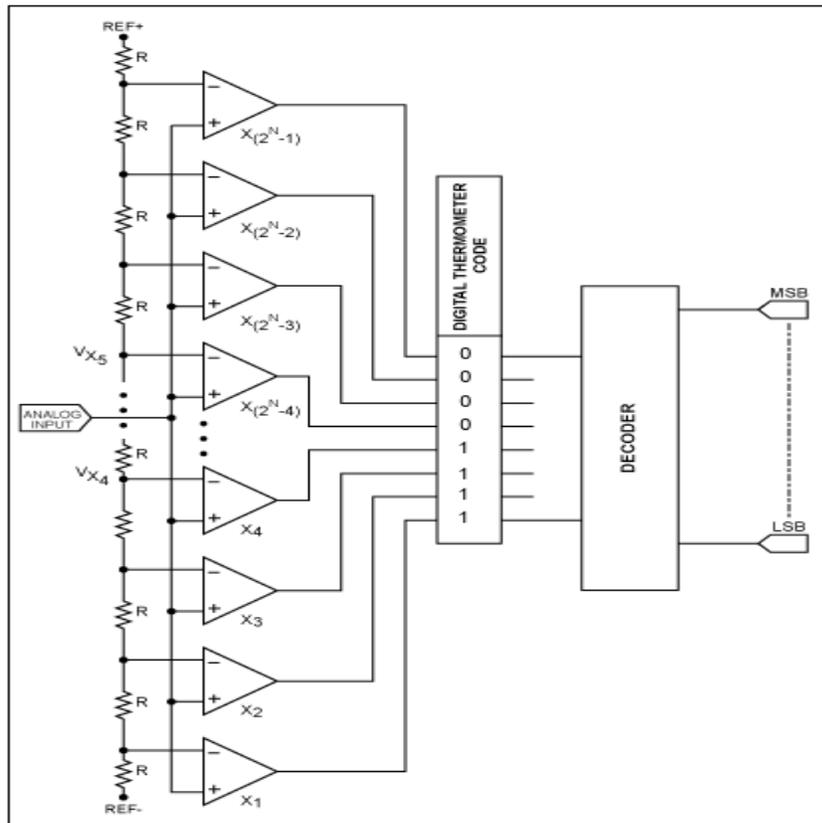
The above block diagram shows the receiver. The receiver section will de-spread the digital signal and then demodulate it.

## ADC

The front end of the transmitter section is the ADC. ADCs of this type have a large die size, a high input capacitance, and are prone to produce glitches on the output (by outputting an out-of-sequence code). Initially we were planning to design a 10-bit ADC but we realized that the speed was not matching the requirements. Hence we implemented a 4-bit ADC.

### Description of the 4-bit FLASH ADC Architecture

Figure below shows a typical flash ADC block diagram. For an "N" bit converter, the circuit employs  $2^N - 1$  comparators. A resistive divider with  $2^N$  resistors provides the reference voltage. The reference voltage for each comparator is one least significant bit (LSB) greater than the reference voltage for the comparator immediately below it. Each comparator produces a "1" when reference voltage applied to it, is higher than its analog input voltage. Otherwise, the comparator output is "0". Thus, if the analog input is between  $V_{x4}$  and  $V_{x5}$ , comparators  $x_1$  through  $x_4$  produce "0"s and the remaining comparators produce "1"s. The point where the code changes from ones to zeros is the point where the input signal becomes greater than the respective comparator reference voltage levels. This is known as thermometer code encoding. The thermometer code is then decoded to the appropriate digital output code.



N bit Flash Analog to Digital converter

### Design Specifications :

4 bit resolution, 100KSamples/S, Fully differential implementation, +1 volt input full scale, AMI 0.6 $\mu$ m -3M,2P,HIGH-RES technology, 1.0W power dissipation.

### Circuit implementation of 4-bit Flash ADC converter:

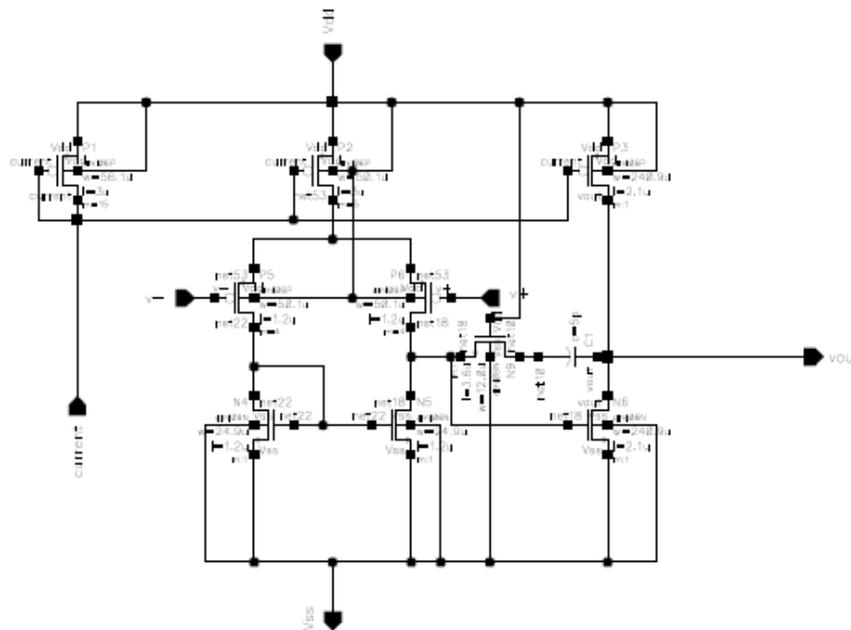
Three key functions performed during this process are: *sampling*, *quantization*, and *reference generation*.

**Reference Generation:** A resistive divider with  $2^N$  resistors provides the reference voltage. The reference voltage for each comparator is one least significant bit (LSB) greater than the reference voltage for the comparator immediately above it.

**Comparators:** The comparators are typically a cascade of wideband low gain stages. They are low gain because at high frequencies it's difficult to obtain both wide bandwidth and high gain. They are designed for low voltage offset, such that the input offset of each comparator is smaller than a LSB of the ADC.

### Design Strategy:

A high-speed opamp should have very high unity gain frequency. We have already designed individually two high speed op-amps in our previous mini-project. We picked the faster one which gave about 75dB at 60Mhz unity gain frequency. The only modification we made was that we changed the width of transistor Q8 to improve the phase margin. With that we were able to meet all of the specifications in simulating the



schematic of our two-stage operational amplifier.2 stage Differential operational amplifier schematic

## **Encoder:**

The encoder logic executes a truth table to convert the ladder of inputs to the binary number output. A regular priority encoder with all its inherent complexity isn't necessary. Due to the nature of the sequential comparator outputs states (each comparator saturating "high" in sequence from highest to lowest) the same "highest-order-input selection" effect may be realized through a set of inverters and 2 input AND logic.

Maximum quantization error could be: Amplitude interval (LSB) =  $A/2^n$

Maximum quantization error: LSB/2

## **DAC**

We designed a simple 4-bit digital to analog converter (DAC) using the R-2R ladder configuration as discussed in chapter 12 of our textbook. We used the same high speed opamp implemented in ADC for DAC. Other design strategies included creating a current switch, determining the value of R in the R-2R ladder, and a current mirror network that replicated the current four times (once for each bit). The current switch was conceived using an inverter and an n-type differential pair. Due to concerns about the size specification we made the width to length ratios of all these transistors small. During the design of the current switch we also opted to change  $V_{SS}$  from -1.2 V as listed in the proposal to -2.5 V. This was done in lieu of taking into consideration the fact that with  $V_{DD} = 2.5$  V and  $V_{SS} = -1.2$  V the output of the inverter would be either -2.5 V or 1.2 V respectively, thus creating a voltage that is less than  $V_{SS}$  and one that is between  $V_{DD}$  and  $V_{SS}$ . We randomly chose the value of 10 k $\Omega$  and  $R_f$  to 20 k $\Omega$  for R and found that this value worked well so we left it unchanged. Our final bias current was 60  $\mu$ A (to increase voltage swing) and it produced an output voltage of 2.36 V.

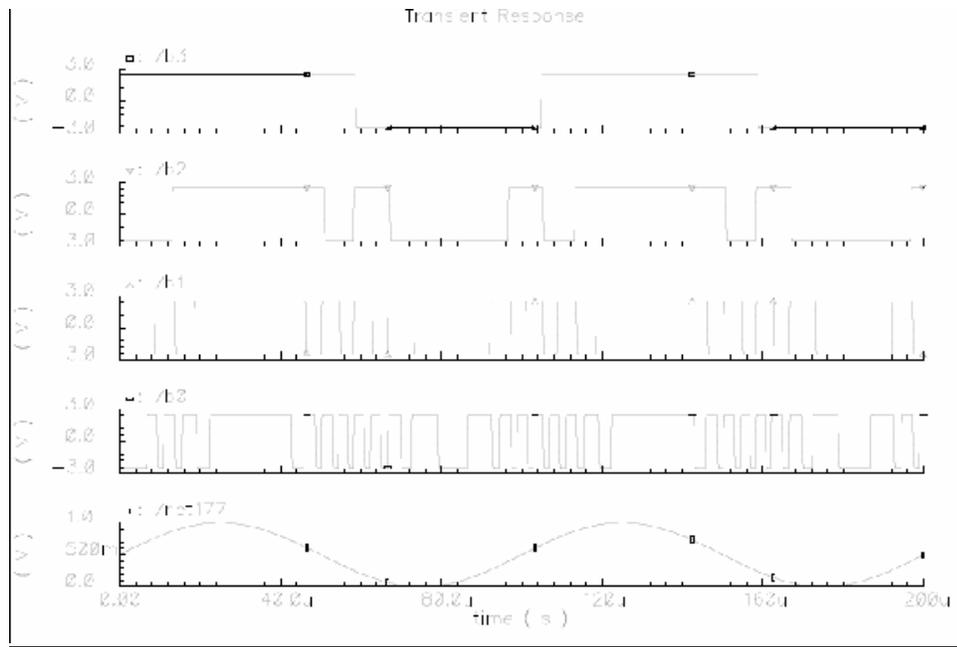
### **Current Switch**

We simulated each part of the circuit individually prior to simulating the entire schematic and finally the layout. To verify the functionality of the current switch we tested it by sending in a pulse input with a bias current of 50  $\mu$ A.

## **Measurement results and circuit performance evaluation:**

### **1) ADC**

We have performed simulation with  $V_{ref} = 1$  volt,  $V_{in}$  (sine wave of .5 volt amplitude, DC offset = .5v, 10KHz frequency) and  $I_{dc} = 250\mu$ A. The simulation results show 4 bit binary value from 4'b0000 to 4'b1111 with the corresponding input change from 0v to 1 volt sine wave. The sampling rate achieved is 320KHz as 10KHz sine wave generates 32 samples in one period.

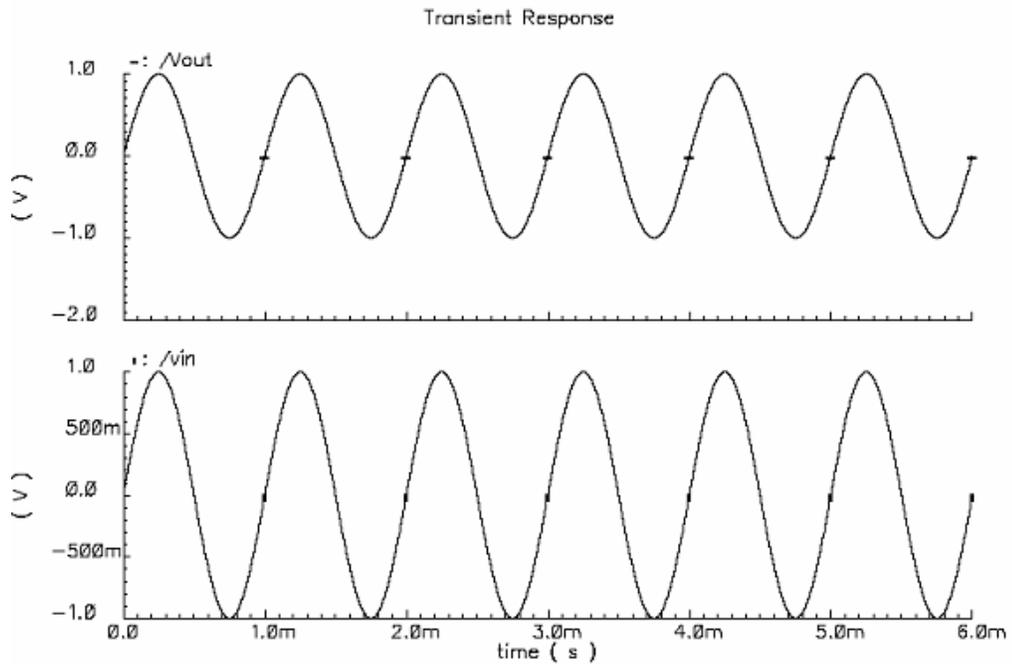


The above figure is transient response of the flash ADC

*Unity-gain buffer:*

Connected the opamp as a basic unity gain buffer and applied a sine wave of 1KHz to the positive input .On running a transient simulation, the output waveform followed the input waveform closely as shown below in figure

Output is in the range **991.496mV** to **-986.408mV** for input in the range of +1V to -1V



### Input common-mode range:

Configured the opamp as unity gain buffer and performed a dc simulation where the input voltage is swept from -2.5V to 2.5V. The input common-mode range of input voltage was determined to be **-2.5V to 2.4998V** as shown in the plot below.

### Output voltage range:

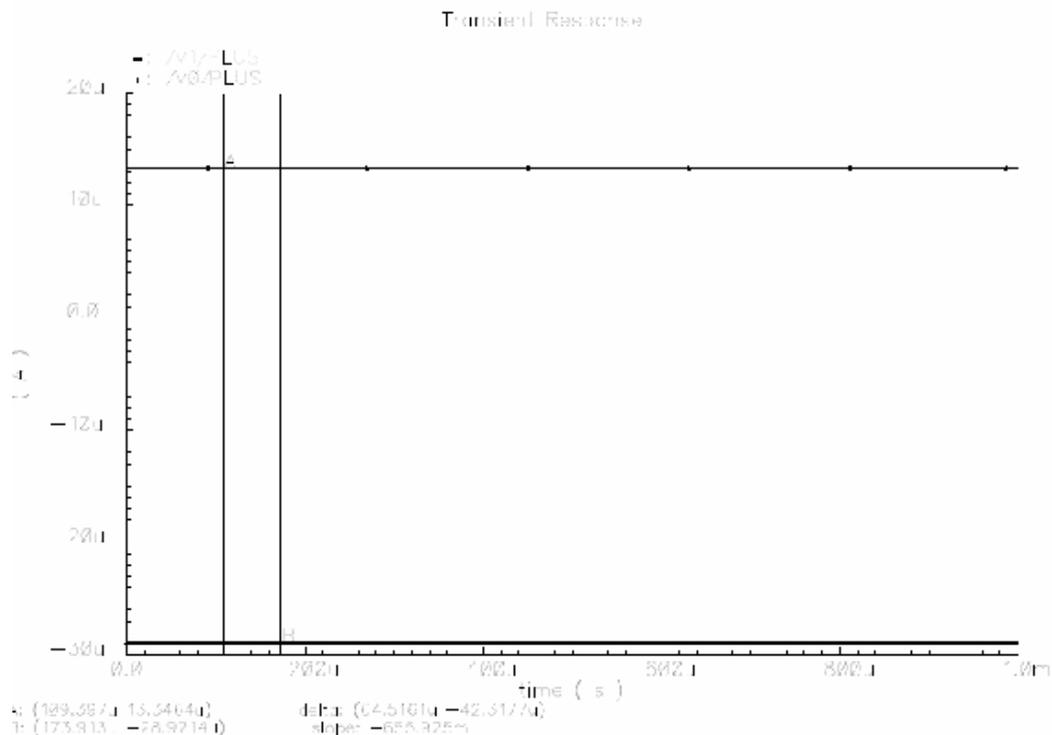
To measure the output voltage range of our opamp, the negative input of the opamp was tied to ground and a dc voltage source was connected to the positive terminal. A DC sweep of this input voltage was performed and the output voltage was seen to swing between **-2.499V to 2.5V**.

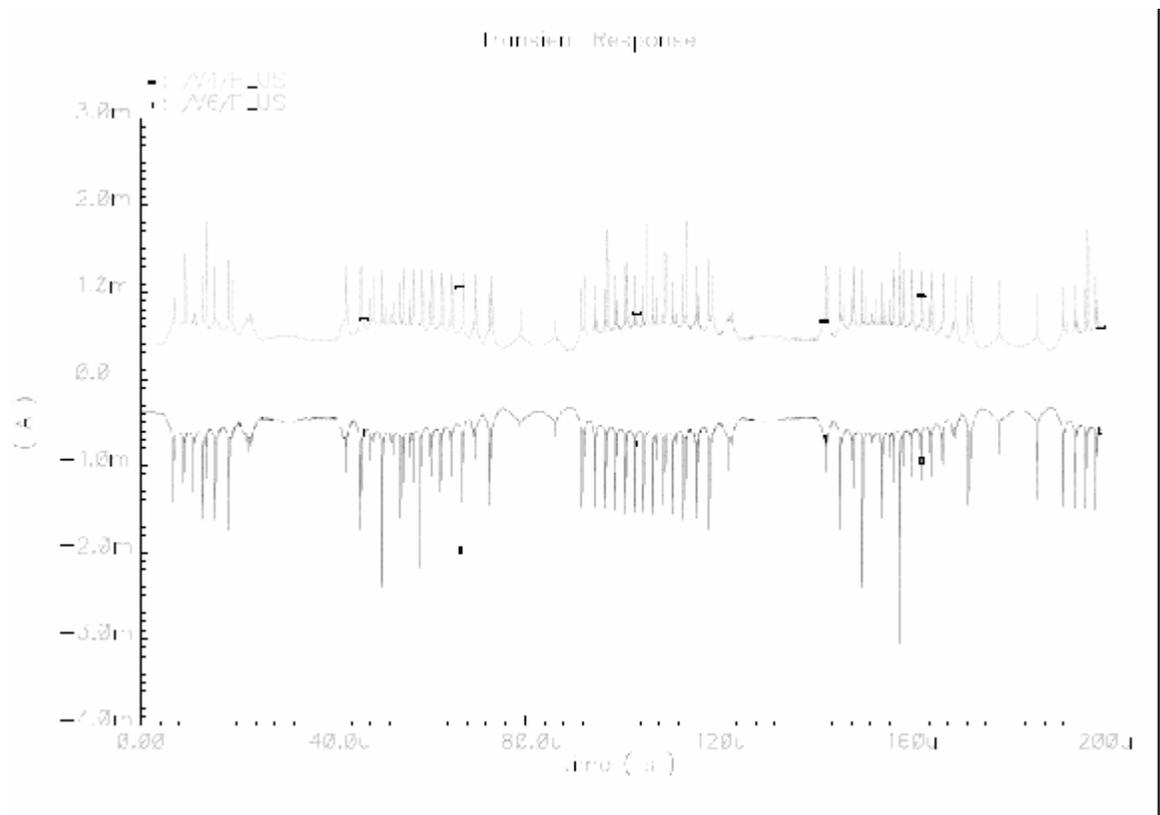
### Input offset voltage:

The DC sweep for above described circuit was performed by sweeping dc voltage from -2mV to 2 mV. The offset voltage observed from the below plot was  $93\mu\text{V}$ .

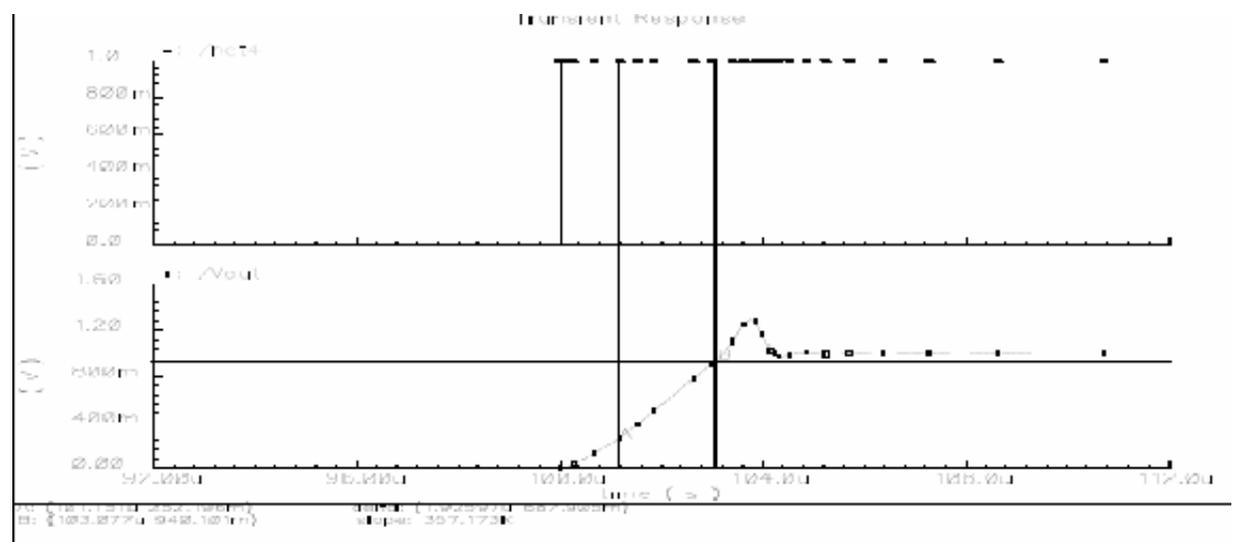
### AC simulation:

The positive terminal of opamp was connected to a sine wave generator in series with the offset voltage DC source. The negative terminal was grounded. On running an AC simulation with frequency ranging from 100Hz to 150MHz, the Bode plots of gain and phase were plotted showing the unity gain frequency and phase margin. The unity gain frequency as seen from the plot is **60.3547MHz**, phase margin is **58.299 degrees** and low frequency DC gain is **75.5397dB**.

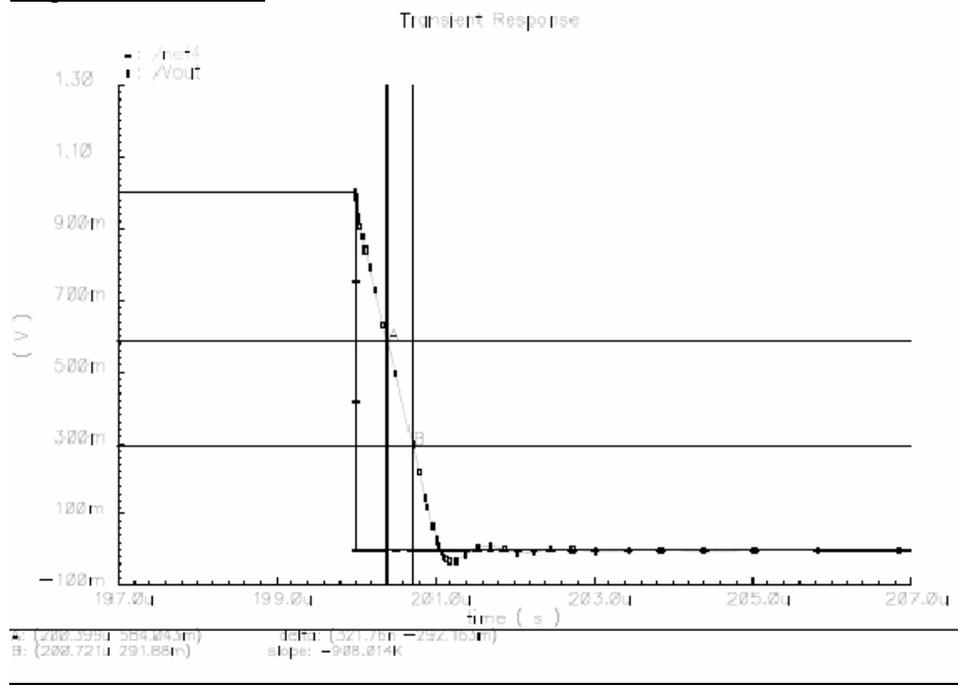




Positive Slew rate:

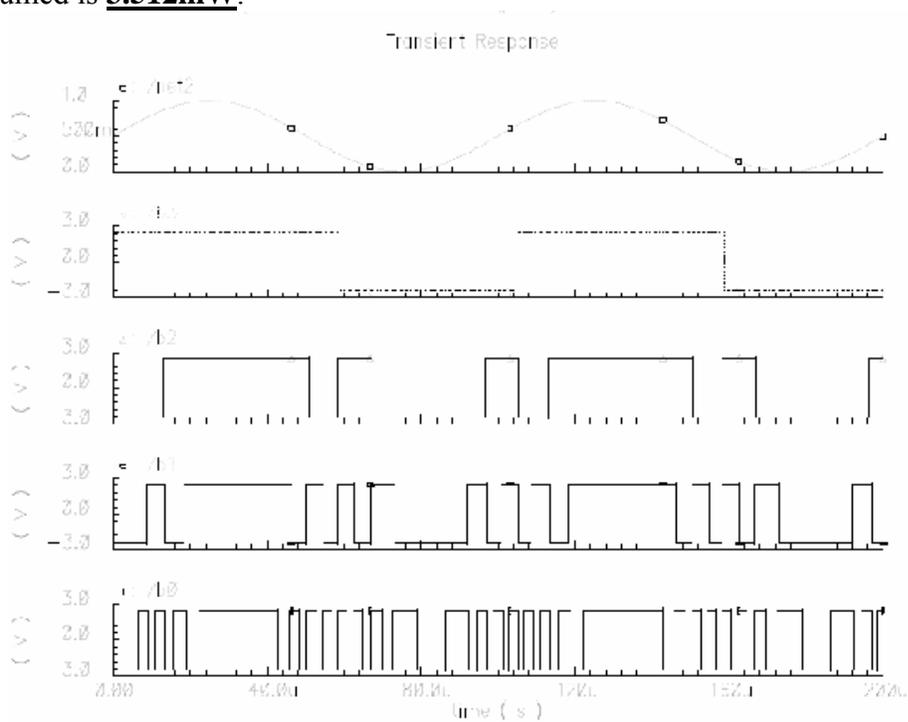


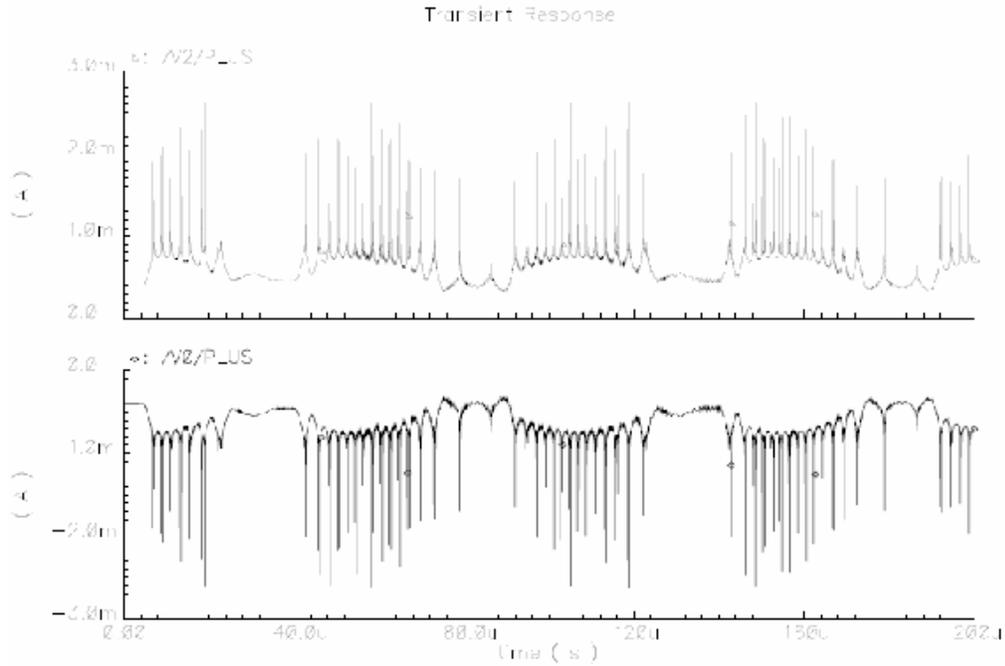
Negative slew rate :



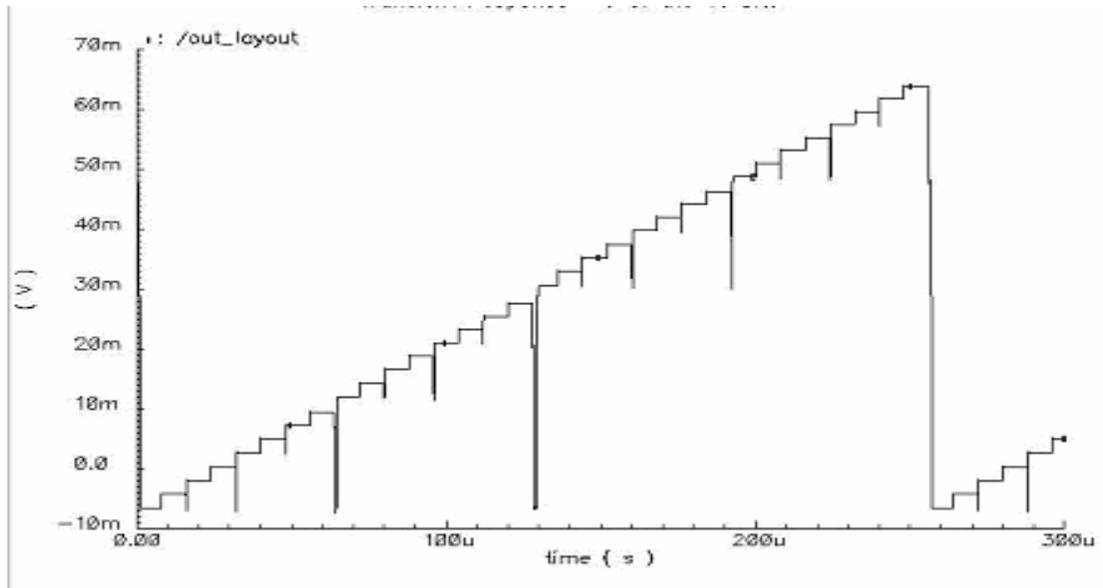
Analog extracted Simulation :

We have performed analog extracted simulation ,which meet the specification of the design. The waveform for the analog extracted simulation are shown below. The power consumed is **3.512mW**.



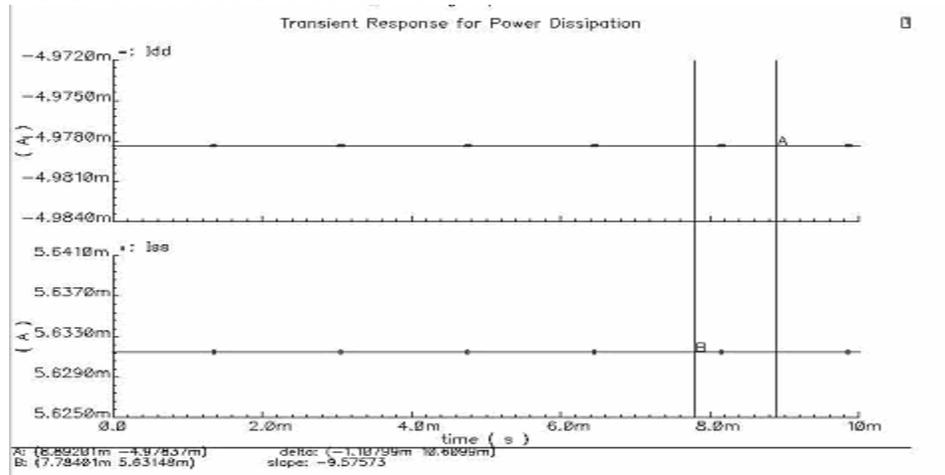


## 2) DAC



In this figure it is easy to see each individual step of the counter. Let it be known that regardless of how big we made the shortest period we were unable to eliminate the abnormally large spike in the center of the waveform. Finally, the amount of power being dissipated was measured. This was done by running a transient simulation and observing the currents flowing from  $V_{DD}$  and  $V_{SS}$  while all the bit inputs were tied to ground.

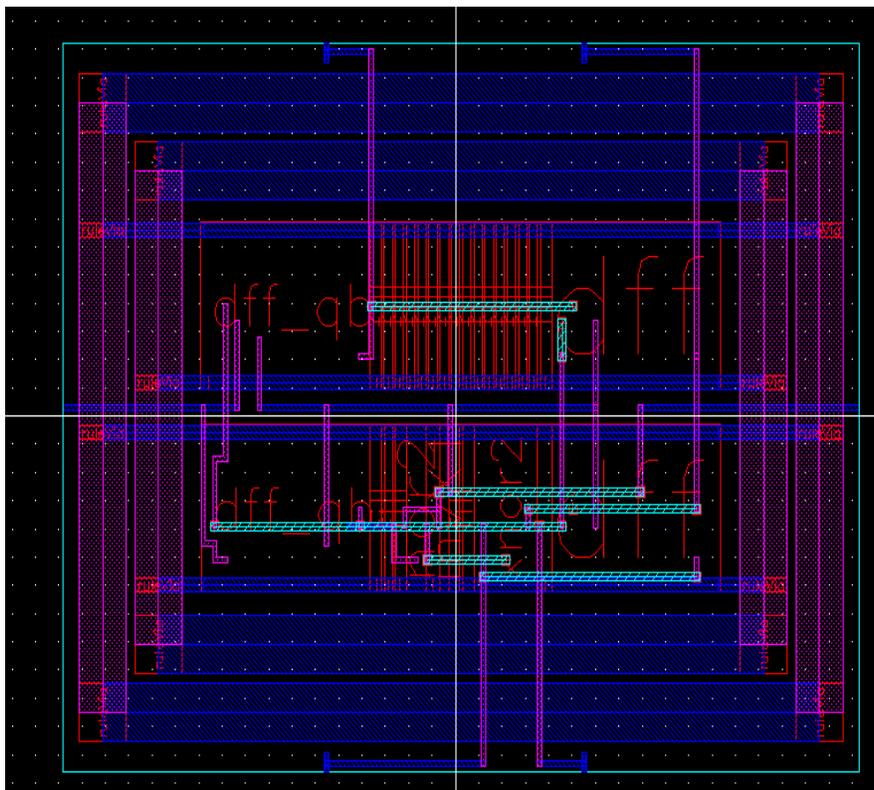
Figure below shows the value of these currents.



The total amount of power that our DAC dissipates is given by the equation  $P = |V_{DD} * I_{DD}| + |V_{SS} * I_{SS}| = 26.5 \text{ mW}$ . Thus we have successfully met all of our required performance metrics listed above.

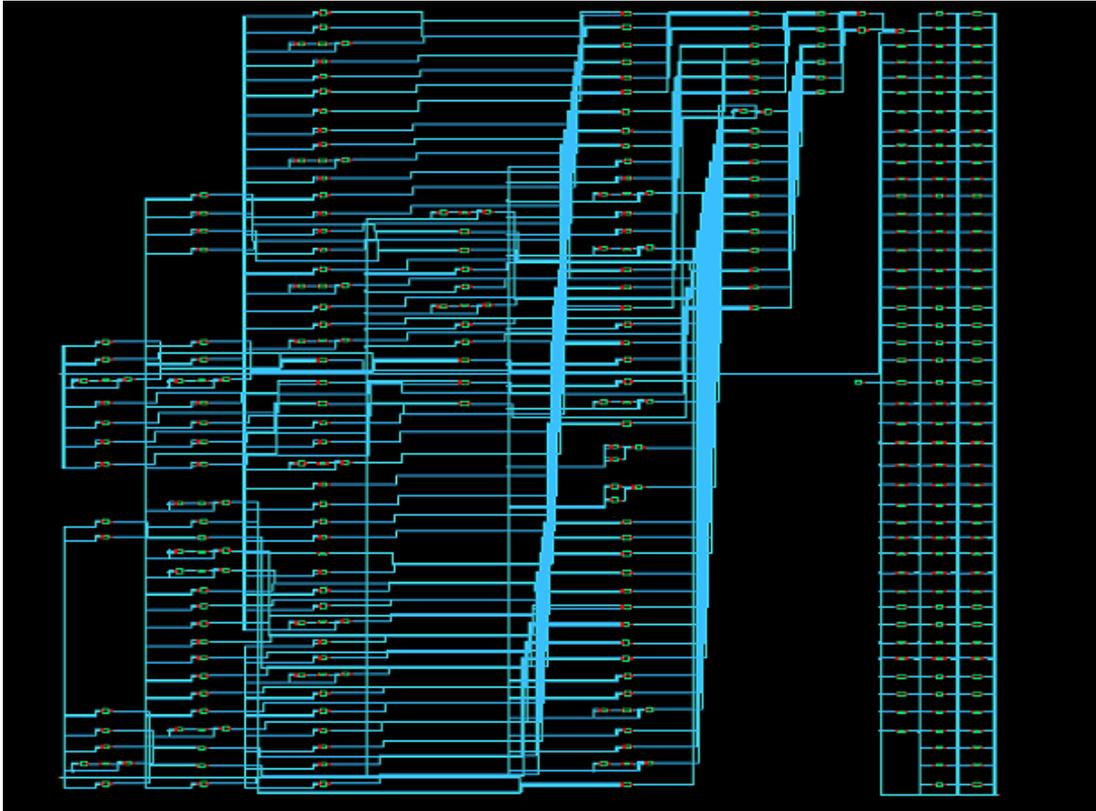
The heart of the system contains Code generator, modulator and Demodulator. The code generator block was created by writing a Verilog code for 4-bit random number generator. Gates in UofU\_Digital were remade with faster switching. The gates that were made NAND, NOR, XOR, MUX and AO4.

A .db file was created for the gates mentioned above. The layout is as shown below.



The modulator block takes 128 bits of data from the ADC and hides it in a random PN sequence. All the data are available simultaneously across the output lines. Again this module was made using Verilog and tested for delay. This system gave a peak delay of 2ns.

The schematic is as shown below:



The layout was generated and LVS obtained.

## PUTTING THINGS TOGETHER:

The transmitter section was implemented by putting the ADC, modulator and code-generator together. The receiver section consists of the demodulator, code-generator and the DAC. The whole system was tested by putting in the receiver with the transmitter.

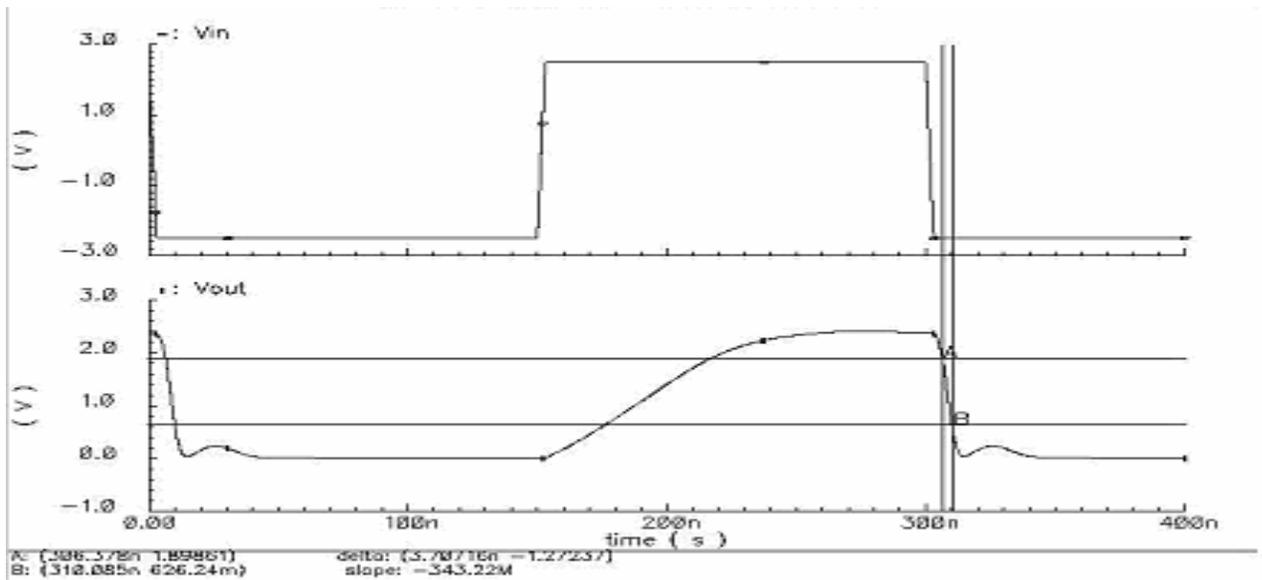
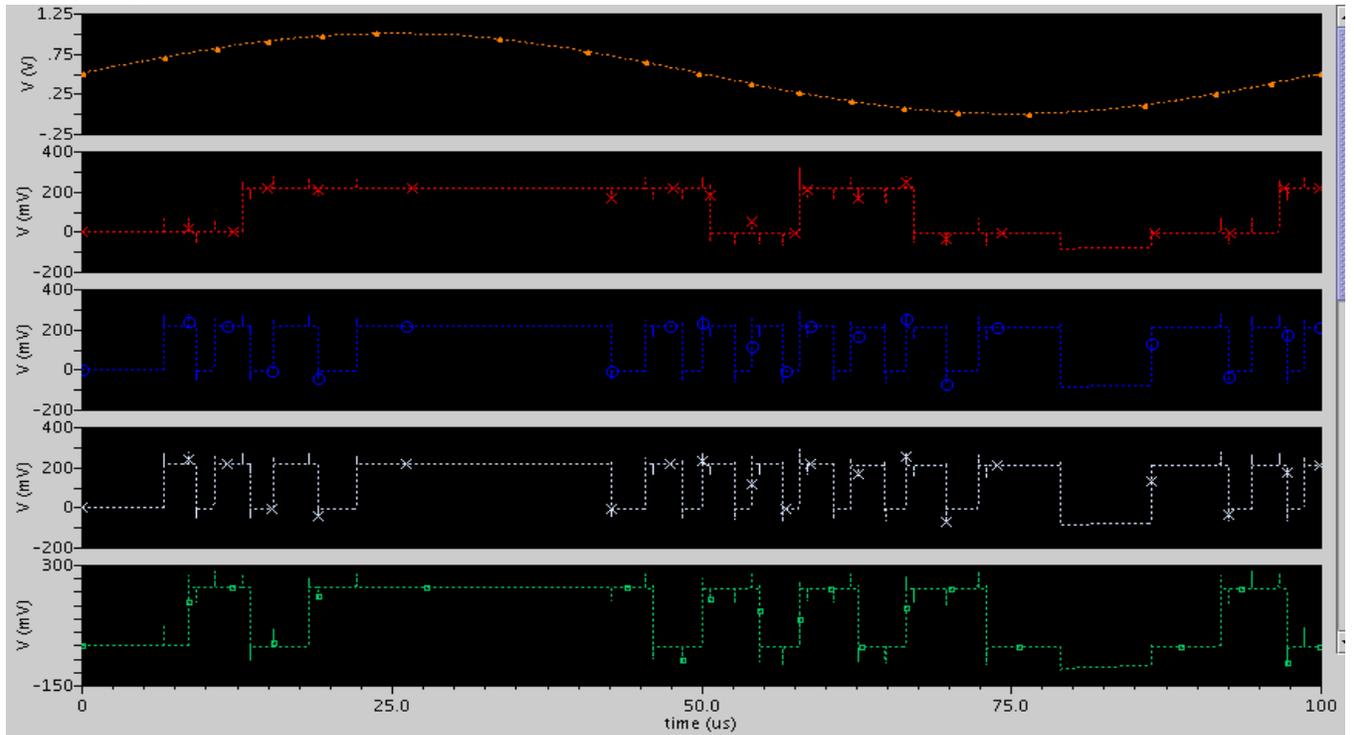
The schematic of the transmitter is shown below:



The above schematic consists of ADC modules on the left hand side along with the code generator.

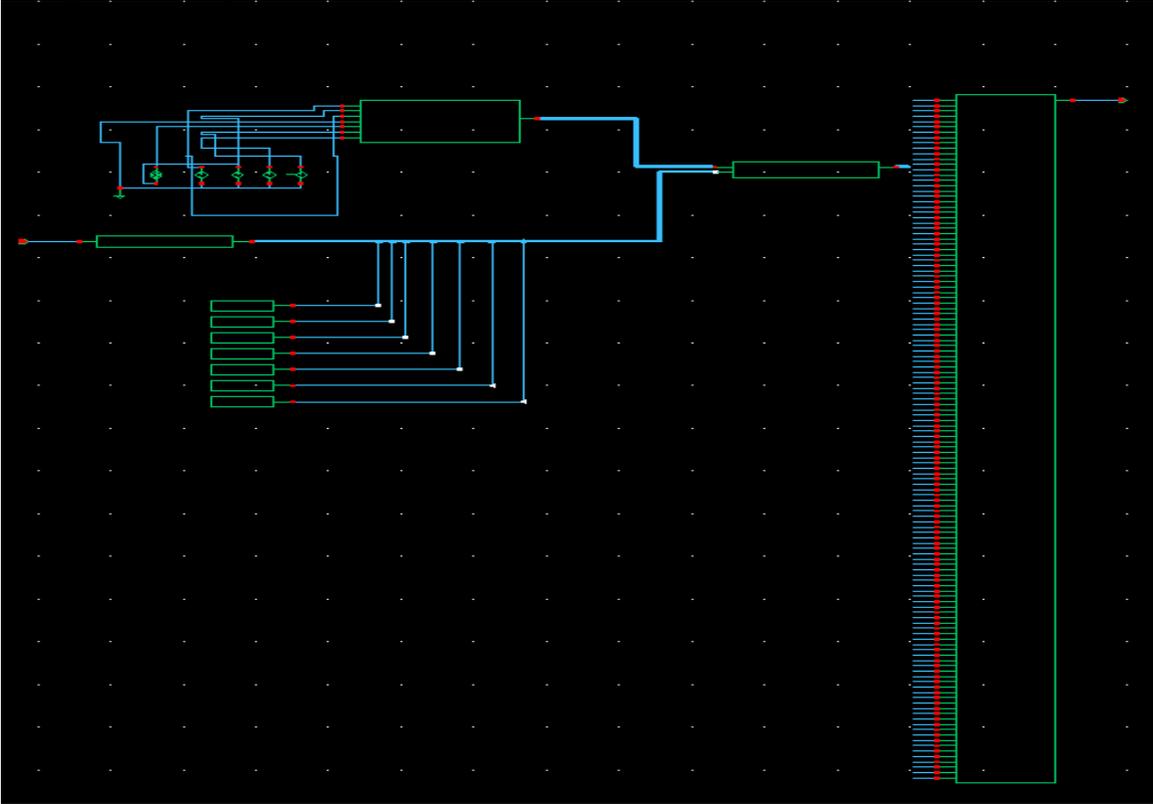
The code generator consists of a sync section. Synch is achieved by having a known sequence as the frame header. The known sequence at the head of the frame is 1675. After this 5555 is used as a marker. Correlation is used to find the frame but this is beyond the scope of chip that we are designing.

## RESULTS

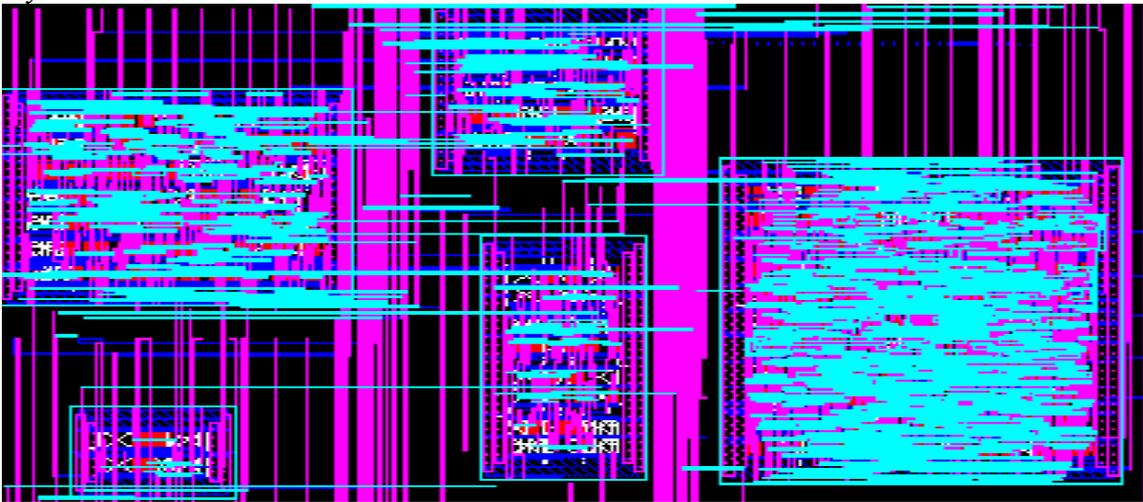


We are showing only four out of 128 bits of the transmitter. Glitches are seen at various points of the graph above. This is because ADC is inherently noisy. More number of bits would probably reduce this problem but they generally are not that fast, hence we have gone for faster and smaller ADCs which are put in series to supply 128 bits of the modulator. If nothing else, they provide multiple data paths for the same set of inputs and hence with this increased redundancy the data error-rate can be brought down by maximizing the number of bits in the same direction.

We were unable to get back our square wave with the proper shape. The delay seems to be higher and shape makes waveform distortion.



layout:-



The results of overall system are given below:

- Power consumed:881mW
- LVS verified
- High simulation time:- 6-7 hrs for 1second test.

- Delay :- 3nS (only for digital side)
- 20% BER :- 30bits flipped.
- Output is noisy.

We could not get the lvs to work for the entire chip. The multiple modules and large number of I/O's threw us off.

### **Testing strategies:**

If we fabricate the chip, then we need to add the pins at each stage so that we can test the signal at the intermediate levels as well. This will help us in debugging the potential failing points in the design. Furthermore, it can help us analyze the characteristics of the different components like transmitter, receiver, op-amps and the functioning of the digital section of the chip that is the encoder. Some of the characteristics that would be interesting to note are the effect of noise on analog section of the chip and the matching of resistors. The whole chip can be fabricated with about 100 pins, 50 pins for each section. A pin or two can be used to study the wire delay in the circuit as this layout does involve long lengths of wires. The other pins can be used to study the characteristics of op-amps used in the chip.

### **CONCLUSION**

All the individual components like ADCs, DACs were designed and tested giving desired results. The whole system was tested and verified by integrating all the components. Also the layout vs LVS check was performed. Golden model verification was done on all the digital blocks.

The system performs almost to specs but we were unable to get all the noise out of the system. As a solution we plan to implement a filter which can probably resolve the noise issues.