Final Design Project
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Abstract
The design of this project is to compare the difference between static and dynamic logic gates. A simple Asynchronous FIFO controller will be used to compare the different performance aspects between the two types of gates. This controller had a small data path of 4 bits wide to bring out the power differences of the two controllers. It was expected that the dynamic FIFO controller would have better performance and power results. All of the comparisons were done using an analog simulator and schematics only. Given the time for the project it was too demanding to complete the layout for the different controller implementations.

Introduction
In the design of different logic styles it is taught that dynamic logic is faster and lower power for Asynchronous designs. They are also supposed to have a much smaller layout area. The purpose of this project is to use a similar logic module and compare the main two different styles of logic gates, static and dynamic. The assumption stated above is that the dynamic logic will outperform the static logic in an asynchronous setting. The logic module chosen was a FIFO controller. This is a small logic block that can take advantage of both types of gates.

The block level design of this test project is a complete FIFO that is three segments deep. Data is sent to a storage device such as a flip-flop or latch and the first signal to be stored will be the first signal to be output. The golden model is also just the data that is input should equal the data output. It has been chosen that the data width will be 4 bits wide.
This was done realizing that modern data paths are often much larger than 4 bits wide. The small data width was chosen to accentuate the power of the FIFO controller and not the power of the data storage devices. To further neutralize the power of the data storage devices all of the inputs were fixed to minimize the line transitions, and further bring out the power of the controllers.

Design
Cadence was used to design all of the schematics. The two FIFO controllers again are asynchronous and the static implementation uses a couple of AND OR INVERT gates with three inverters and a NOR gate for feedback (See Figure 1). The dynamic gate uses two footed NAND domino gates 3 inverters and a NOR gate used for feedback (Figure 2).

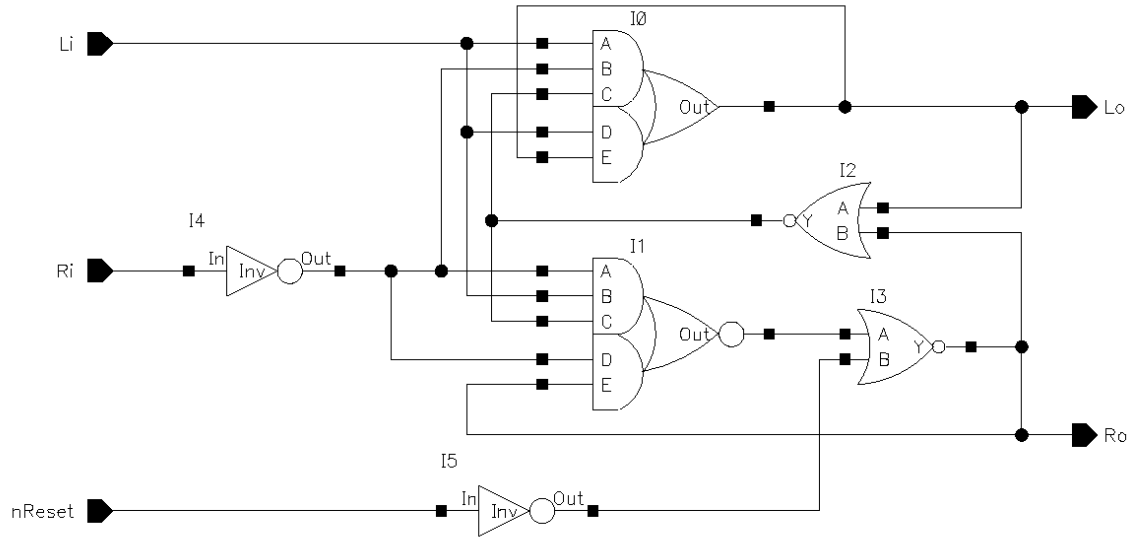

Figure 1 - Static FIFO Controller

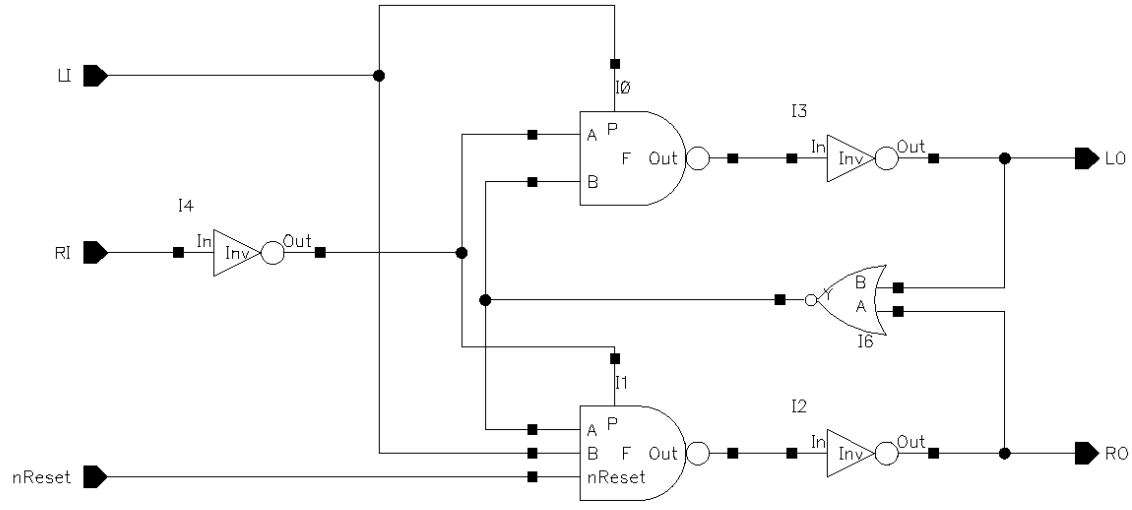

Figure 2- Dynamic FIFO Controller

Both controllers use the same inverter and NOR gate (See Figure 3).

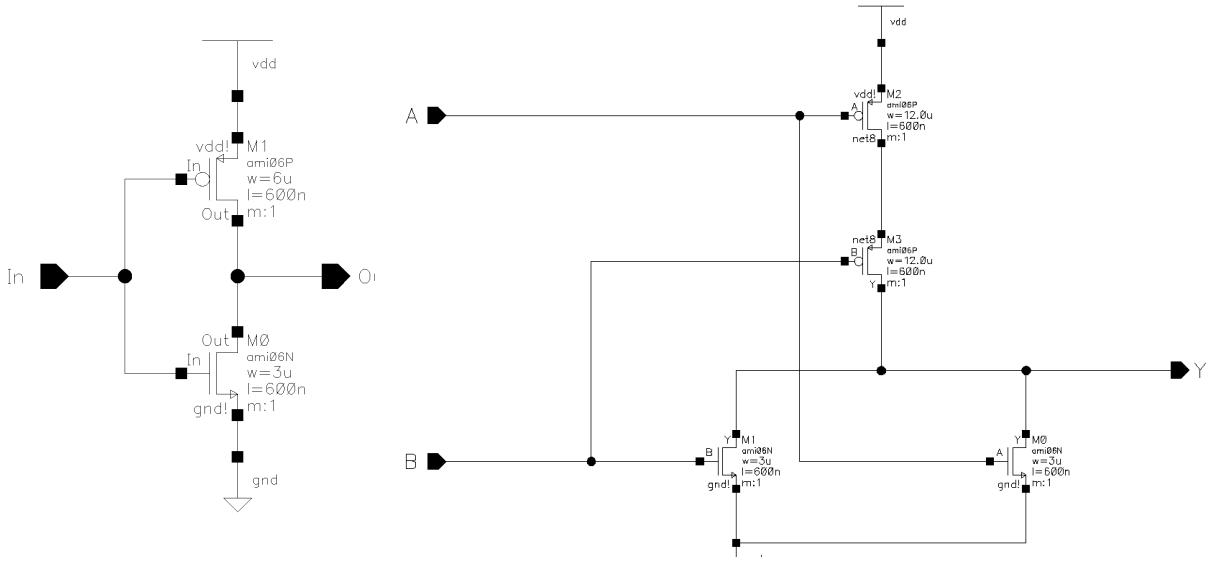

Figure 3 – Left – Used Inverter, Right – Used NOR gate.

The design of the static controller (see Figure 1) uses two custom designed complex logic gates. The first is an AND-OR gate (see Figure 4) and the second is an AND-OR-Invert gate (see Figure 5) with the only difference being that an inverter is on the output of the AND-OR gate. It also incorporates a NOR gate after the AND-OR-Invert gate so that a reset could be used to set the right out (RO) signal to a known good value.

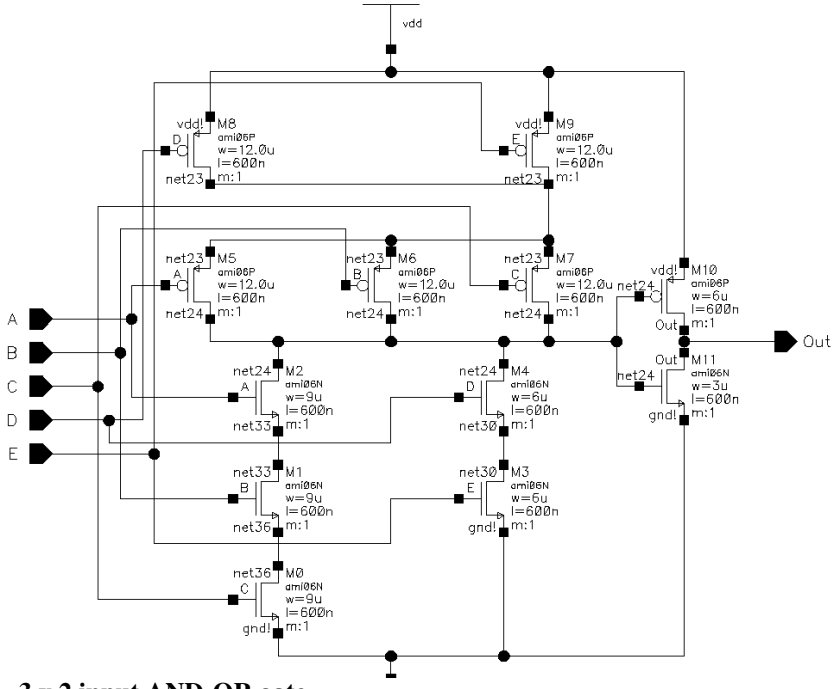

Figure 4 - 3 x 2 input AND-OR gate

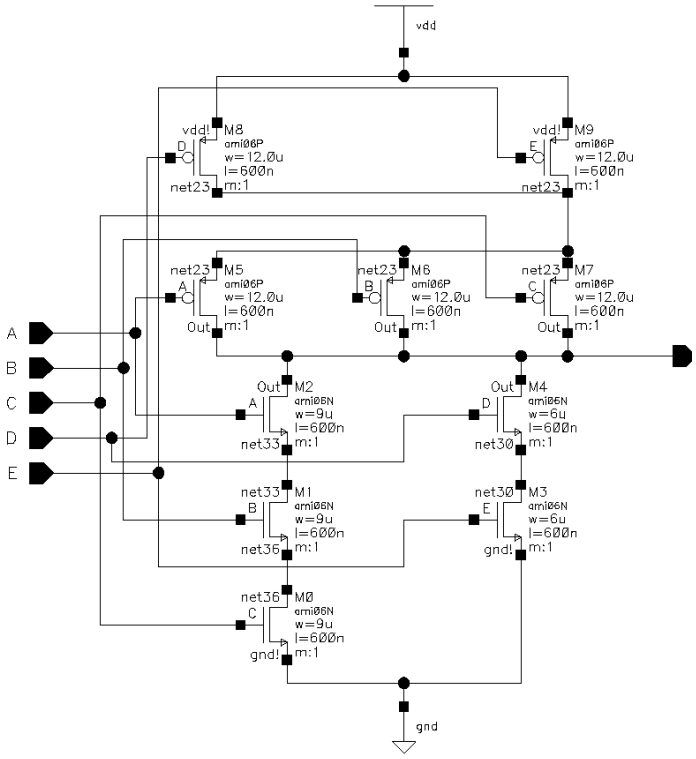

Figure 5 – 2 x 3 AND-OR-Invert gate.

The design of the dynamic controller (see Figure 2) also employed two custom designed gates. Both are 2 input footed domino gates, the first being a standard domino gate (see Figure 6) and the second (see Figure 7) includes a reset line that allows the controller to be reset to a known default state.

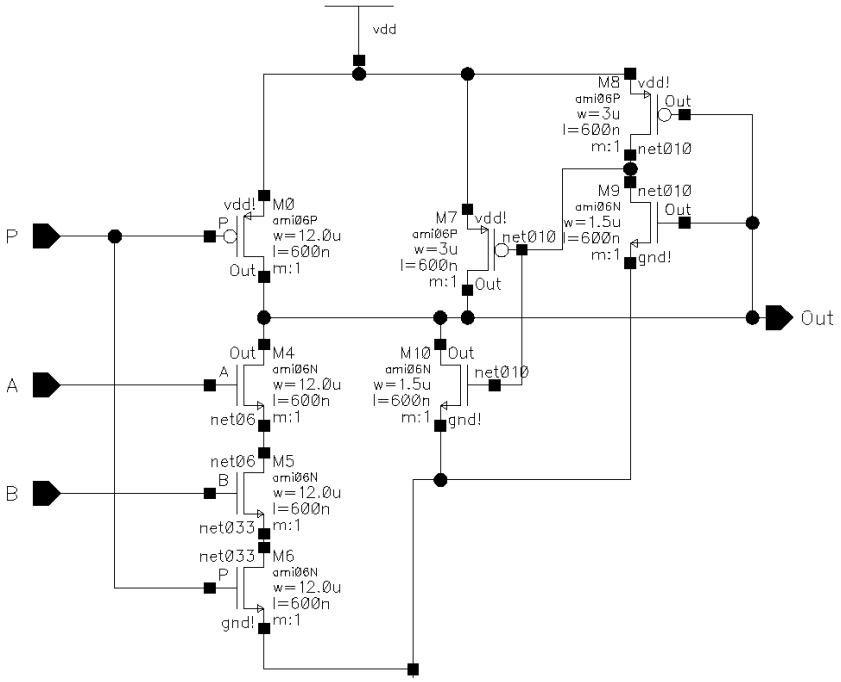

Figure 6 – 2 Input Footed Domino Gate.

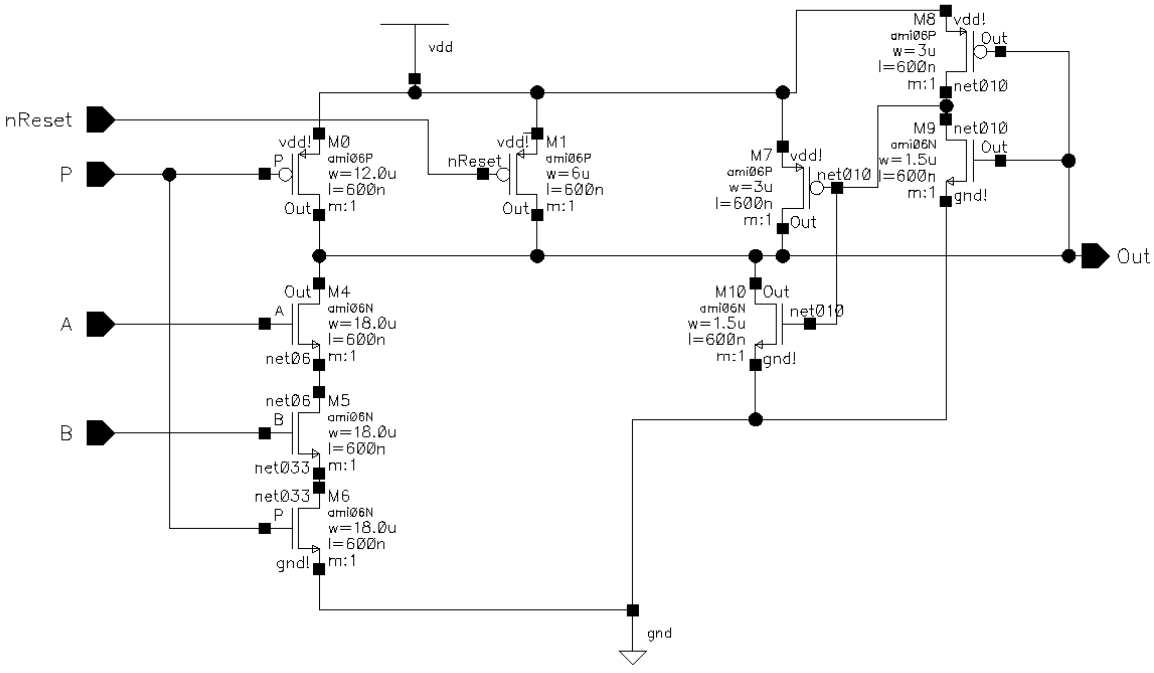

Figure 7 – 2 Input Footed Domino Gate With A Signal to Reset The Output High

From an initial analysis of this design the dynamic controller has 27 total transistors and the static controller has 34. Not only does the dynamic have fewer transistors but it also has only one set of stacked p-mos transistors in the NOR gate where the static controller has one in every gate except for the inverters. This will limit power and further reduce the area used.

Analysis

The Analysis was started using the spectra simulator in cadence and this simulator had some limitations and so hspice was then used for some measurements. The timing specs and plots were done using spectra, and the power measurements were done using hspice with a netlist generated by cadence.

The simulation was done with a 200n seconds transient analysis. This was done with both the static and dynamic controllers. To make the FIFO continuously run the reset signal was connected to the left input of the first controller, and the left output was fed through an inverter into the left input. The third controller right output was taken through two inverters and fed back into the right input. So once the reset signal is low and then rises the FIFO will continue to run. During the 200nS simulation the static FIFO had 54 complete FIFO transitions (see Figure 8)

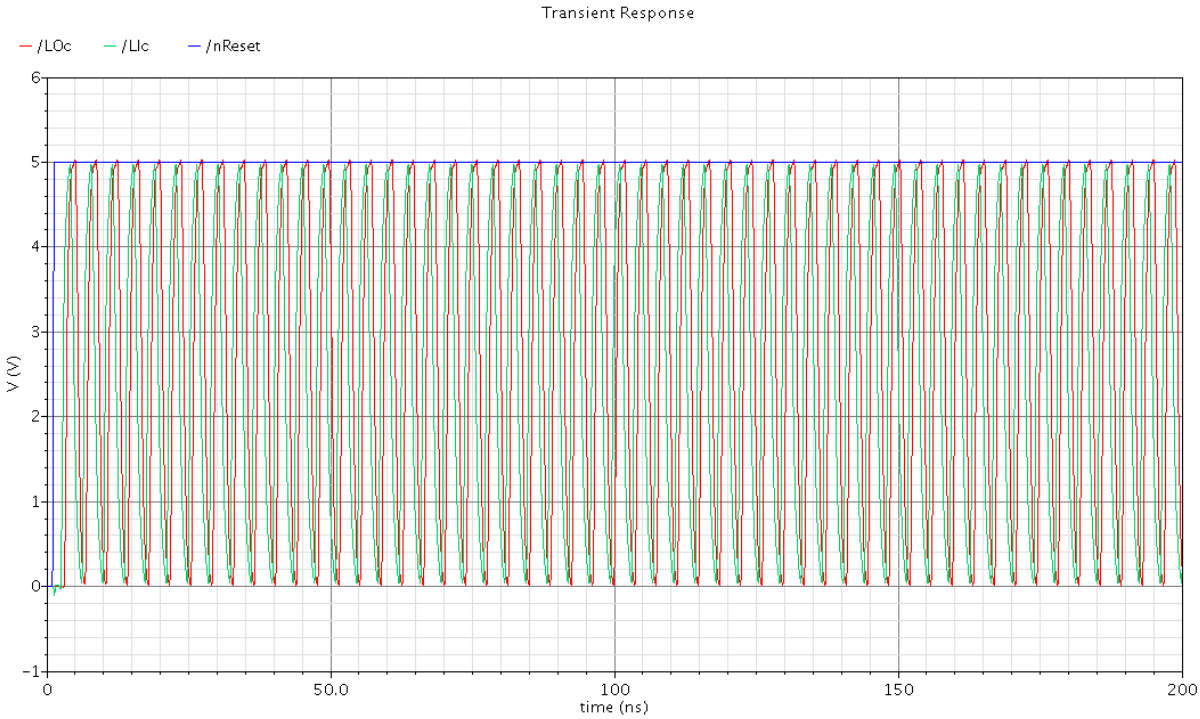

Figure 8 – Transient Response From the Static FIFO Controller

Each FIFO cycle had a period of 3.73nS. The total power used for this simulation is 27.9m watts. The power per cycle was 516uW.

The Dynamic FIFO had the following results. It had a total of 82 complete FIFO cycles (see Figure 9). Each cycle period was 2.4nS. The total power used for the entire simulation was 33.9mW. The power used per each cycle was 413uW.

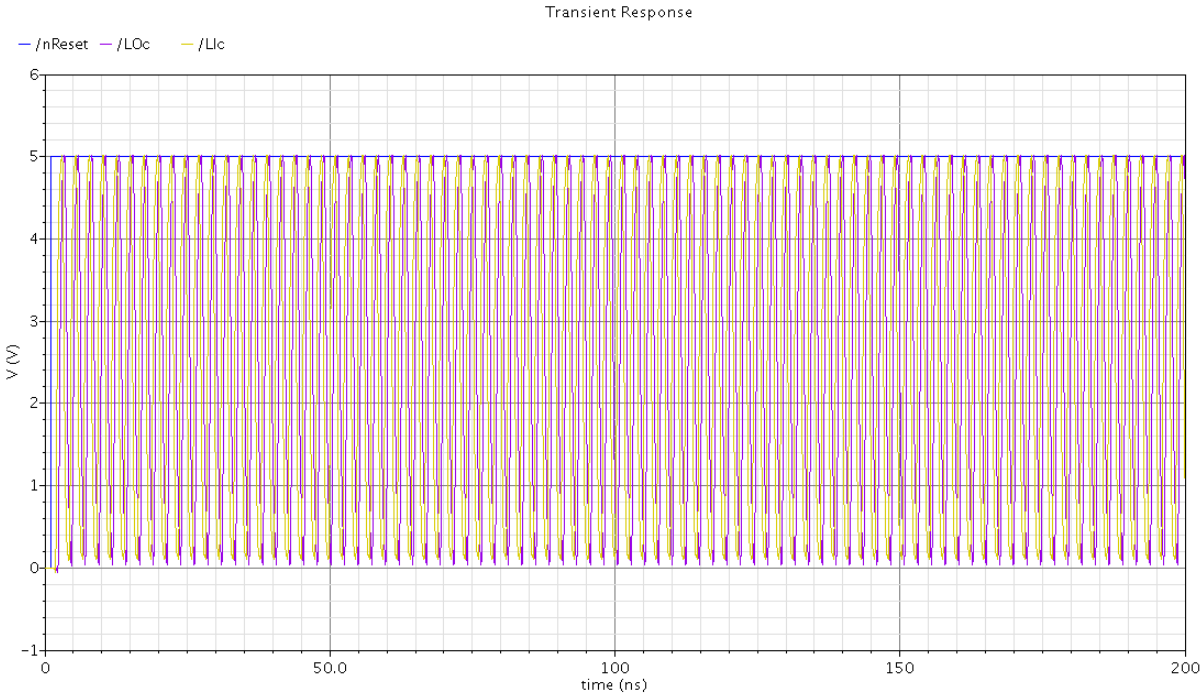

Figure 9 – Complete Transient Response For the Dynamic FIFO

Conclusion

The initial assumption made was that the Dynamic FIFO controller would be faster and use less power, along with less area. From the simulations run in this project it was determined that the dynamic FIFO used less power, 413uW per cycle vs. 516.7uw. The speed advantage was determined to be the dynamic FIFO as well, 2.4nS vs. 3.73nS. With the dynamic FIFO using 7 fewer transistors it also has the smaller size. According to the above-mentioned simulation an asynchronous FIFO controller using dynamic gates is a superior design.