Call For Abstracts
2012 IEEE/ACM Workshop on CAD for Multi-Synchronous and Asynchronous Circuits and Systems

November 8th, 2012 Hilton San Jose, CA USA Co-located with ICCAD

Background

Many current integrated circuit designs are partitioned into multiple timing domains, allowing each domain to be independently optimized for power and performance. This simplifies timing closure and enables the integration of IP blocks with different timing requirements. One system approach is to use traditional handshaking circuits naturally employ locally generated timing signals that can yield high performance or provide fine-grained activity gating for low power. GALS methods where the asynchrony appears at the level of system integration are another approach.

Multi-synchronous and asynchronous architectures present design challenges and require supportive CAD that arise when departing from the timing methodology and determinism of single frequency synchronous designs. While the departure is already well underway, more systematic CAD support for these designs promises lower power, higher robustness, and better performance. Such a new generation of CAD also enables a much wider base of designers to exploit these advantages.

This workshop provides a forum to discuss current challenges of asynchronous design, how to address the CAD problem, and how to gain penetration of this disruptive technology in industry. This is intended for both technical and industry experts in the asynchronous, GALS, elastic-pipelining, and latency insensitive design communities.

Key Topics

- Current state of the art in asynchronous design
- Timing closure, optimization and validation
- Physical design of asynchronous circuits
- Challenges for multi-synchronous/asynchronous design
- Process variation and its role in multi-synchronous design
- Synthesis and system architecture
- Addressing the test challenge
- The role of asynchronous design in multi-clocked designs and DVFS
- Perspectives for/from commercialization
- Solutions to key challenges to asynchronous commercialization

Technical Program Committee

Co-Chairs: Ken Stevens, University of Utah & Mark Greenstreet, University of British Columbia

John Bainbridge, Sonics	Gary Delp, Mayo Clinic
Jo Ebergen, Oracle	Steve Furber, University of Manchester
Mike Kishinevsky, Intel	Rajit Manohar, Cornell
Marc Renaudin, Tiempo IC	

Format

Two page maximum in US Letter or A4 format. **One page is strongly recommended.** Once accepted, the authors are required to give a 20 minute presentation as well as provide a poster for discussion and interaction. There will also be time provided for round table discussions on the topics.

Timeline

Submission Deadline:	Sep. 24th, 2012
Notification of Acceptance:	Oct. 1st, 2012
Workshop Date:	Nov. 8th, 2012

Submission

Please send the abstract in PDF format to kstevensece.utah.edu with subject "MSCAS Submission"

Contact

Please contact Ken Stevens, ECE Department, University of Utah, kstevensece.utah.edu for questions.