Estimating MTBF of Multi-Stage Synchronizers

D. Zar\textsuperscript{1}, T. Chaney\textsuperscript{1}, J. Cox\textsuperscript{1}, S. Beer\textsuperscript{2} and R. Ginosar\textsuperscript{2}

\textsuperscript{1}Blendics, Inc., St. Louis, Missouri,
\textsuperscript{2}EE Dept., Technion-Israel Institute of Technology, Haifa, Israel
Synchronizers Essential in Multi-Synchronous SoCs

- Low-skew, global clock trees problematic
- Survey of proposed SoC design starts*
  - 32% contain > 50 clock domains
  - 12% contain > 100 clock domains
- Each CDC requires reliable synchronization

* Survey by Graham Bell, Director of Marketing, Real Intent, Inc. See:
Old Rules of Thumb* Unreliable

• Problematic because of increases in
  – Clock speeds
  – Data rates
  – Number of CDCs
  – Semiconductor process variability
  – Tau (low power $\rightarrow V_m \sim V_t$)
• FO4 no longer predicts $\tau$
• Negative temperature coefficient of $V_t$

* Two FFs in cascade are almost always enough, but when you are worried, use three.
Determining Synchronizer MTBF

• Intrinsic parameters - vary with PVT
  – Settling time-constant $\tau_{\text{eff}}$
  – Number of stages $n$
  – Aperture width $T_W(n)$

• Extrinsic parameters - vary with application
  – Clock rate $f_C$
  – Data transition rate $f_D$
  – Duty cycle $\alpha$
Determining Synchronizer Parameters

• Physical measurements $\rightarrow$ protracted testing
  – Testing at PVT corners $-$ impractical number of runs
  – Testing multi-stage synchronizers $-$ interminable

• Circuit simulation $\rightarrow$ automated, pre-fab testing
  – Synchronizer standard-cell designer specifies:
    • Intrinsic parameters: $\tau_{\text{eff}}, n, T_W(n)$
  – Synchronizer standard-cell integrator specifies:
    • Extrinsic parameters: $f_C, f_D, \alpha$
  – MTBF formula for a multi-stage synchronizer needed
Over the years, many ways to estimate MTBF in multi-stage synchronizers have been presented in the literature. Here are three common forms:

- Kinnement, Altera and others: MTBF\( (n) \) is proportional to waiting \( n \) times as long. (2007)
- Gabara, et al: master and slave latches have independent \( T_W \). (1992)

\[
MTBF_{Kinniment}(n) = \frac{\exp[nT_C/\tau]}{T_W f_D f_C}
\]

\[
MTBF_{Kleeman}(n) = \frac{\exp[(nT_C-nt_p)/\tau]}{T_W f_D f_C}
\]

\[
MTBF_{Gabara}(n) = \tau \frac{\exp[(nT_C-2nt_s^S)/\tau]}{T_W^2 f_D f_C}
\]
Simulation vs. Measurement

- Simulating with *MetaACE*, we compared a latch $\tau$ with measurements on a 65 nm, low-power circuit ($\tau \pm 5\%$).
Some MetaACE results

Output of First Flip-Flop

Output of Second Flip-Flop
Comparison of MTBF Results

MTBF Calculation Methods for a 4-Stage Synchronizer Based on Identical Master-Slave Flip-Flops (IBM 90 nm, -1 σ, -40 C, 1.1 V)
Published Formulas Conservative

- Existing formulas treat inter-stage coupling conservatively
- Voltage traces leaving metastability
  - $V_N$ is voltage range that covers invalid, next-stage outputs.
  - $V_L$ is voltage range that covers invalid, last-stage outputs.

- For multi-stage synchronizers $V_L << V_N$ and as a result MTBF based on $V_L$ can much greater than that based on $V_N$
- Therefore must simulate entire synchronizer
Estimation of MTBF by Formula

Blendics MTBF Calculation for Multi-Stage Synchronizers Based on Master-Slave Flip-Flops (IBM 90 nm, -1 σ, -40 C, 1.1 V)

\[
MTBF(n) \geq MTBF_{Blendics}(n) = \frac{\exp \left[ \frac{nT_C}{\tau_{eff}} \right]}{T_W(n)f_Df_C}
\]

\[
\frac{1}{\tau_{eff}} = \frac{1}{2} \left( \frac{1}{\tau_M} + \frac{1}{\tau_S} \right)
\]

4 flip-flops

3 flip-flops

2 flip-flops

Simulated

Calculated

Blendics Inc.
Predicting Synchronizer MTBF Important

• More multi-synchronous SoC designs
• Low-voltage circuits increase $\tau$
• Low-temperature operation increases $\tau$
• Semiconductor variability increases failure risk
• Failures hard to recognize in silicon
  – Must have accurate MTBF before fab
  – MTBF can be calculated from $\tau_{eff}$, $n$ and $T_w(n)$
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