Figure 3.1. Logic values as voltage levels.

Figure 3.2. NMOS transistor as a switch.

Figure 3.3. PMOS transistor as a switch.

Figure 3.4. NMOS and PMOS transistors in logic circuits.

Figure 3.5. A NOT gate built using NMOS technology.

Figure 3.6. NMOS realization of a NAND gate.
Figure 3.7. NMOS realization of a NOR gate.

Figure 3.8. NMOS realization of an AND gate.

Figure 3.9. NMOS realization of an OR gate.

Figure 3.10. Structure of an NMOS circuit.

Figure 3.11. Structure of a CMOS circuit.

Figure 3.12. CMOS realization of a NOT gate.
Figure 3.13. CMOS realization of a NAND gate.

Figure 3.14. CMOS realization of a NOR gate.

Figure 3.15. CMOS realization of an AND gate.

Figure 3.16. A CMOS complex gate.

Figure 3.17. A CMOS complex gate.

Figure 3.18. Voltage levels in a CMOS circuit.
### Figure 3.19. Interpretation of voltage levels.

<table>
<thead>
<tr>
<th>$V_x$</th>
<th>$V_{out}$</th>
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</thead>
<tbody>
<tr>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
</tr>
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#### (a) Voltage levels

<table>
<thead>
<tr>
<th>$x_1$</th>
<th>$x_2$</th>
<th>$f$</th>
</tr>
</thead>
<tbody>
<tr>
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<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
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</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

#### (b) Positive logic truth table and gate symbol

<table>
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<th>$x_1$</th>
<th>$x_2$</th>
<th>$f$</th>
</tr>
</thead>
<tbody>
<tr>
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</table>

#### (c) Negative logic truth table and gate symbol

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<th>$f$</th>
</tr>
</thead>
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<td>1</td>
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</tbody>
</table>

### Figure 3.20. Interpretation of voltage levels.

#### (a) Voltage levels

<table>
<thead>
<tr>
<th>$x_1$</th>
<th>$x_2$</th>
<th>$f$</th>
</tr>
</thead>
<tbody>
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<td>1</td>
<td>1</td>
</tr>
<tr>
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#### (b) Positive logic

<table>
<thead>
<tr>
<th>$x_1$</th>
<th>$x_2$</th>
<th>$f$</th>
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</thead>
<tbody>
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</table>

#### (c) Negative logic

### Figure 3.21. A 7400-series chip.

#### (a) Dual-inline package

#### (b) Structure of 7404 chip

### Figure 3.22. Implementation of $f = x_1x_2 + x_2x_3$.

### Figure 3.23. The 74244 buffer chip.

#### Pin Layout

#### Figure 3.24. Programmable logic device as a black box.

#### Logic gates and programmable switches

#### Inputs (logic variables)

#### Outputs (logic functions)
Figure 3.25. General structure of a PLA.

Figure 3.26. Gate-level diagram of a PLA.

Figure 3.27. Customary schematic of a PLA.

Figure 3.28. An example of a PLA.

Figure 3.29. Output circuitry.

Figure 3.30. A PLD programming unit.
Figure 3.31. A PLCC package with socket.

Figure 3.32. Structure of a CPLD.

Figure 3.33. A section of a CPLD.

Figure 3.34. CPLD packaging and programming.

Figure 3.35. Structure of an FPGA.

Figure 3.36. A two-input lookup table (LUT).
Figure 3.37. A three-input LUT.

Figure 3.38. Inclusion of a flip-flop with a LUT.

Figure 3.39. A section of a programmed FPGA.

Figure 3.40. A section of two rows in a standard-cell chip.

Figure 3.41. A sea-of-gates gate array.

Figure 3.42. An example of a logic function in a gate array.
Figure 3.43a. NMOS transistor when turned off.

Figure 3.43b. NMOS transistor when turned on.

Figure 3.44. Current-voltage relationship in the NMOS transistor.

Figure 3.45. Voltage levels in the NMOS inverter.

Figure 3.46. Voltage transfer characteristics for the CMOS inverter.

Figure 3.47. Parasitic capacitance in integrated circuits.
Figure 3.48. Voltage waveforms for logic gates.

Figure 3.49. Transistor sizes.

Figure 3.50. Dynamic current flow in CMOS circuits.

Figure 3.51. Poor use of NMOS and PMOS transistors.

Figure 3.52. Poor implementation of a CMOS AND gate.

Figure 3.53. High fan-in NMOS NAND gate.
Figure 3.54. High fan-in NMOS NOR gate.

Figure 3.55. The effect of fan-out on propagation delay.

Figure 3.56. A noninverting buffer.

Figure 3.57. Tri-state buffer.

Figure 3.58. Four types of tri-state buffers.

Figure 3.59. An application of tri-state buffers.
Figure 3.60. A transmission gate.

Figure 3.61a. Exclusive-OR gate.

Figure 3.61b. CMOS Exclusive-OR gate.

Figure 3.62. A 2-to-1 multiplexer built using transmission gates.

Figure 3.63. An example of a NOR-NOR PLA.

Figure 3.64. A programmable NOR plane.
Figure 3.65. A programmable version of a NOR-NOR PLA.

Figure 3.66. A NOR-NOR PLA used for sum-of-products.

Figure 3.67. PAL programmed to implement two functions.

Figure 3.68. Pass-transistor switches in FPGAs.

Figure 3.69. Restoring a high voltage level.

Figure P3.1. A sum-of-products CMOS circuit.
Figure P3.8. The pseudo-NMOS inverter.

Figure P3.9. A gate-array logic cell.

Figure P3.10. Circuit for problem 3.54.

Figure P3.11. Circuit for problem 3.55.