Administrative Notes:
1. E-mail list: anyone willing to be added, come talk to me.

2. Note's office hours time & location:

3. Assigned readings: skip stuff not mentioned in class,
   if not mentioned in class or on assignments:
   pretty safe to skip it.

4. Write lecture notes: on open paper, or scan them later.

Recap from last class:
1. Qualitative look at PLL operation
2. Linear PLL analysis:
   - assume PLL is locked, blocks are all linear (approximation)
   a. Simple case for loop filter
      - Type 0, 1st order PLL
      - stability, transient response, phase error
   b. Low pass (lag) filter
      - Type 0, 2nd order PLL
      - revisited standard second-order equation form
      - pick up with that...

Recall from last time: for one pole low pass filter: \( E(s) = \frac{K_{PE}}{1 + s/\omega_{pp}} \)

- Subbing into previously developed expression for closed loop transfer function:

Open loop: \( \alpha(s) = K \)

\( \frac{1}{1 + s/\omega_{pp}} \) \( \leq \) 2nd order

\( T_{type \ 1} \)

\( H(s) = \frac{K}{s^2 + s + K} \) characteristic equation for the PLL

- We standard form for characteristic equation:

\( s^2 + 2\zeta \omega_n s + \omega_n^2 \)

\( \zeta \) natural frequency

\( \zeta \) damping factor

- Review of red arrow in previous day's notes.
So, we have:

\[
G(s) = \frac{K}{s(1 + \frac{1}{s\omega_p})} \quad \text{\(K = k_{pp}, k_{pp}, k_{pp}\)}
\]

\[
H(s) = \frac{K}{s^2 + \omega_n^2 + \frac{2\zeta\omega_n}{s} + \frac{1}{s} + K}
\]

\[
\text{Filter gain (only if we have a curve implementation)}
\]

For analysis, we will borrow from control theory and express this in terms of natural frequency \(\omega_n\) and damping factor \(\zeta\).

General form:

\[
s^2 + as + b \equiv s^2 + 2\zeta\omega_n s + \omega_n^2
\]

(Review your control theory text if necessary)

This allows us to determine the loop dynamics in terms of these values.

\(\omega_n\) gives an indication of the bandwidth (but actual 3dB bandwidth will vary depending on the value of \(\zeta\)).

\(\zeta\) gives an indication of the stability for low \(\zeta\), the transient response will exhibit ringing (\(\zeta\) is related to phase margin). We usually design for \(\zeta\) between 0.5 and 2, with 0.707 (\(\frac{\pi}{4}\)) being a preferred value (critically damped = \(\zeta = 1\), no ringing).

\[\omega_n = \sqrt{\omega_p K}\] and \[\zeta = \frac{1}{2\sqrt{\omega_p K}}\]

(Note: \(\omega_n\) and \(\zeta\) are only defined for second order loops.)

\[
H(w) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}
\]

Small \(\zeta\) (under-damped)

LARGE \(\omega_n\) (over-damped) Step Response: A

Small \(\zeta\) (under-damped)

Frequency response:

Observe that we have 2 quantities to alter, \(K\) and \(\omega_p\). There are 3 parameters we would like to set to determine the loop characteristic: \(\omega_n, \xi\) and the DC gain \(K\) (for steady state phase error) among other things. So, we need additional degrees of freedom.

Note: for \(\zeta \geq 0.707\), no peaking in \(H(s)\), makes this useful for telecom application (such as repeaters) because no zeros in the TF.
- Transient response will be similar to that for the type 1 first order PLL, but the transient response may exhibit ringing.

For phase error response:

\[ K \text{eq} E(s) = \frac{1}{1 + G(s)} \quad \text{also} \quad E(s) = 1 - H(s) \]

\[ = \frac{s(s + 2\zeta\omega_n)}{s^2 + 2\zeta\omega_n s + \omega_n^2} \]

- Ch 6 of the book gives example responses for phase error and output phase for various input functions and damping factor.

- Acts as normalized to \( \omega_n \), as it is a rough indication of the bandwidth.

- They are easy to calculate, just multiply the input function by the transfer function and take the inverse L.T., as we did for the simple Type 1, 1st order case.

- The book differentiates between the type of loop filter in that analysis by adding a parameter \( \zeta = 0 \) for the rampail filter.

- I have never seen this treatment else so we will not use it in class, but it is not very complicated, easy to understand if you read the book.

- Stability: Make Bode plot for open loop T.F. \( G(s) \):

- Like the first order PLL examined previously, the ideal Type 1, second order PLL is unconditionally stable, as phase margin approaches \(-180^\circ\) but never reaches it.

- However, how the phase margin is of importance, as it can lead to ringing in the step response of peaking in the frequency response.

- For very low phase margins, non-linearities could push it over the edge to instability.

- Also, for a real PLL, there will be higher order parasitic poles, so at high frequencies the phase will in fact be less than \(-180^\circ\).
Recall the design has the disadvantage; that we only have two control knobs (K and \( \omega_p \)), but there are 3 parameters we want to set.

For example, we usually want \( \zeta = \frac{1}{2} \) for an optimally flat freq response.

Now \( \frac{1}{\sqrt{2}} = \frac{\omega_n}{\omega_p} \Rightarrow K = \frac{\omega_n}{2} \).

Now we wish to set \( \omega_n \) to fix settling time \( T_s \) and bandwidth:

\[
\omega_n = \sqrt{\omega_p K}
\]

\[
\Rightarrow \omega_p = \frac{\omega_n^2}{K}
\]

Now, sub \( 2 \) into \( 1 \):

\[
K = \frac{\omega_n}{\sqrt{2}}
\]

So, we see that we cannot adjust \( K \), which we would like to do to get steady state phase error and the capture range (as will be discussed later).

\[ \text{Solution: Use a lead-lag filter to gain an extra degree of flexibility} \]

Now:

\[
E(s) = \frac{K \omega_p}{(s + \frac{\omega_n}{\sqrt{2}})(s + \frac{\omega_n}{\sqrt{2}})}
\]

\[ \text{S: Open-loop TF:} \]

\[
G(s) = \frac{K \omega_p}{s(s + \frac{\omega_p}{\sqrt{2}})}
\]

\[ \text{Typical, 2nd order,} \]

\[
H(s) = \frac{K \omega_p(s + \frac{\omega_n}{\sqrt{2}})}{s^2 + \frac{\omega_p}{\sqrt{2}} s + \omega_n^2}
\]

Again, cast it in terms of the standard form for the 2nd order denominator:

\[ \omega_n = \sqrt{K \cdot \omega_p} \] (as before)

\[
\zeta = \frac{1}{2} \left( \frac{\omega_p}{\omega_n} + \frac{\omega_n}{\omega_p} \right)
\]

(different than for the lag filter).

Now we have sufficient degrees of freedom to independently specify all three of

For phase error transfer function, the bandwidth, damping, and DC gain:

\[
E(s) = 1 - H(s) = \frac{s(s + \omega_p)}{s^2 + 2\zeta \omega_n s + \omega_n^2}
\]
- Response to different inputs can again be plotted using the multiplication of Laplace transform technique.
- While plotting a number of these responses is well.
- For the block's notation, this corresponds to the variable of being between 0 and 1.

Stability: Draw the Bode plot:

- Still unconditionally stable.
- Zero brings about an increase in the phase so this can enhance the stability (phase margin).
- Also zero gain step has greater...

- Transient responses are generally similar to the case for the lag filter.

- Adding the zero has two side effects:
  1) Increases the bandwidth (remember the expression for \( \omega_n \) was altered, adding an extra term.
  2) The gain frequency gain does not fall off as quickly, which can be troublesome for some applications (increased attenuation of high frequencies by the loop filter).

- This is an improvement over the lag filter but we still have a non-zero phase error for a frequency step.
- We can see this by going through the math again using \( G(s) \) or intuitively, because for a frequency step at the \( s^2 \) output of \( G(s) \), the output voltage must change by \( \frac{\Delta U}{K_u} \).求出相位误差来计算由 \( \Delta U \)引起的相位误差

- In many applications this is undesirable.
How can we eliminate the phase error?

- We just said that the phase error was given by \( \omega \).
- So the phase error will be zero if any of the denominator quantities are infinite at \( \omega \).
- This can be achieved by adding an integration to the loop filter.

**Simplest way to do this:** make the LTP a pure integration (with some gain)

\[ \begin{align*}
& F(s) = \frac{K}{s} \\
& G(s) = \frac{K}{s^2 + K} \quad \text{Type 2, 2nd order}
\end{align*} \]

\[ \begin{align*}
E(s) &= 1 - H(s) = \frac{s^2}{s^2 + K} \\
E(0) &= 1 - \frac{K}{s^2 + K} = \frac{s^2}{s^2 + K}
\end{align*} \]

Observation: poles of \( H(s) \) are at \( s = \pm j \sqrt{K} \) (on the imaginary axis).
- As poles in the LTP indicate instability, this means that by a slight perturbation, the system will become unstable.

We can also show this with the Bode plot:

- Clearly, this is unstable.

Q: How can we make it stable?
A: Add a zero to the open loop T.F. to decrease the phase margin at the cross over frequency

New Bode plot:

- We can see the system is now stable (if the zero is placed properly).
second order loop filter of a type n loop (n > 1) must contain at least n-1 zeros, or the loop will be unstable.

So, by adding a zero to our integrator filter, the resulting filter is called an integrator & lead filter, or alternatively a P+I (proportional and integral) filter in control theory.

Integrate & Lead Filter

\[ H(s) = \frac{K(s)}{s(1+\frac{s}{\omega_n})} \]

\[ G(s) = K \left( \frac{1}{\omega_n s} \right) \]

\[ s^2 + \frac{2\zeta \omega_n s + \omega_n^2}{\omega_n^2} \]

\[ \omega_n = \sqrt{K} \]

\[ \zeta = \frac{1}{2\sqrt{K}} \]

\[ \text{These are both very different than they were for the log & log-log filters!} \]

\[ \text{Err: } TF = \frac{s^2}{s^2 + 2\zeta \omega_n s + \omega_n^2} \]

Responds to different input (a again be plotted in the same manner as previously.

Significantly, we find that for a frequency step, the phase error settles out to zero.

Again, these responses are plotted in Ch. 6 of the text.

- Let us now look at the zero log-log term phase error for a frequency step:

- Third-domain signal waveform:

\[ x(t) \rightarrow \text{Integrator} \rightarrow y(t) \]

\[ v_o(t) \rightarrow v_h(t) \rightarrow v_c(t) \rightarrow y(t) \]

\[ \text{Increase frequency of } x(t) \text{ at this point} \]

\[ \Delta \phi = 0 \]

\[ \text{New control voltage is held by integrator} \]
Stability: We have already drawn the bode plot, like all 2nd order PLLs it is unconditionally stable, with a phase margin determined by the placement of the zeros.

Observation: The absence of phase error is very desirable, the big advantage to this configuration.

- Some gain peaking will always occur for this configuration due to the 2 zeros (at very low frequencies).
- It is also the case for the lead-lag filter, which also has a zero.
- As mentioned, in some applications this is problematic.
- Also referred to as "jitter peaking" because it can increase the phase noise (or jitter) of a signal.

\[ \text{Signal} \times \text{PLL Transfer Function} = \text{After PLL} \]

- As we will see in the following discussion on phase-detectors, the integration performed in the loop filter can also be accomplished using a specific type of phase detector (PFD) along with a charge-pump.

Higher Order PLLs

- You will rarely see a PLL with type > 2, but many applications require higher order PLLs.
- As mentioned previously, the higher frequency poles are usually neglected in the initial design, for the loop dynamics, but these cannot be included in later simulations since they do have an impact.
- See Fig. 6.14 on page 127 of the Egan text (Section 6.12) for an illustration of the impact of higher order poles.
- Care must also be taken to assure stability, as the added poles reduce the phase margin.
- Some reasons to include additional poles:
  - To increase the rolloff at high frequency offsets if the PLL is being used as a jitter.
  - To filter out more of the periodic disturbance on the VCO control voltage, like caused by the periodic phase detector output. (As we will see, this periodic disturbance leads to "spurs" in the output spectrum.)
That is most of the S-domain analysis we will have to do, now we will move on to looking at some of the specifics of implementing each of the blocks we have looked at, starting with... Phase Detectors.

Actually, before we discuss phase detectors, let us define one other concept, so it will be useful to think of the different types of phase detector with respect to this.

**Tracking Range (also called Hold Range)**

- For a slowly varying input frequency, how far can the PLL output track the input frequency? (This is defined as the tracking range).

This is usually determined by the non-linearities in the phase detector or VCO characteristics.

Illustration:

\[
\begin{array}{cccc}
\Phi_i & + & K_{pd} & \Phi_e \\
\hline \\
\text{LPF} & \text{F}(s) & K_{vco} & \text{Out} \\
\end{array}
\]

For a input key step \( \Delta u \), recall \( \Delta u = \Delta \Phi_e \) for a type 1 PLL.

\[
\begin{align*}
K_e &= K_{pd} \cdot K_{vco} \\
\Delta u &= \Delta \Phi_e \cdot K_{pd} \cdot K_{vco} \\
V_{ppb} &= \text{output voltage of phase detector} = V_{pp} \\
V_{ppb} &= \text{non-linearity} \\
K_{pp} &= \Phi_e \\
\text{Input} \Phi_i \\
\end{align*}
\]

- \( \Delta u \) is limited by \( V_{ppb} \) or determined by the linear range of the phase detector, as we will see, this differs for different phase detectors.

- Could also be limited by clipping at loop filter output, depending on \( K_{pp} : \frac{\Phi_e \cdot K_{pd} \cdot K_{vco}}{\text{loop filter output}} \)
Finally, can be limited by the linear range of the VLO, if further
increases in Vout do not bring about a further increase in frequency

![Frequency Limiting](image)

The above discussion assumed a Type 1 PLL.

**Q:** For a Type 2 PLL, which of the PD, LPF, or VLO will most
limit the tracking range?

**A:** Only the VLO will limit the tracking range, due to integration in the
loop filter (although clipping by the loop filter could also occur).

### Stability for a Type 1 PLL:

\[ \Delta \text{Phase} = \Delta \text{Freq} \times \text{KPD} \times \text{KLPF} \times \text{KLO} \]

- Closed-loop gain at DC
- (assuming the phase detector is the limiting factor)
- Otherwise, it is determined by loop filter clipping on non-linear VLO
  characteristics.

Now, review with Phase Detectors...

As we review various phase detectors, there are a few relevant things to
consider for each design:

1. What is the input phase error (DE) range for which the characteristic
   is monotonic (we saw this relates to the tracking range)?
2. What is the response to unequal input frequencies (freq. detection,
   false locking)?
3. How do the input amplitude and duty cycle affect the characteristic?

**D. Multiplier Phase Detector:**

- **Q:** Why is this called a multiplier? How about a MOSFET circuit?

- Drawn on the left is a Gilbert cell
- Implemented using BJTs, but can also be created using MOSFETS (I can help you with
  this if you want to use it for the project)
- For small signals at A and B, this circuit
  acts as a multiplier
- Any "mixture" type circuit will work as a
  phase detector of this nature.