EF 536: Lecture 4
Jan. 12, 2006

Administrative Items:
1. HW #1 due today
2. New grading rules on blank paper so they are easier to read
3. HW #2 assigned (only made 5 copies)
4. Switch office hours to 11:30-12:30

Recap from last class:
1. Finished linear PLL analysis:
   a. low-pass (lag filter): type 1, 2nd order
   b. lead-lag filter: type 1, 2nd order (more flexible)
   c. integrate and lead filter: type 2, 2nd order (no phase error)

2. PLL tracking range

3. Started analysis of PLL building blocks: Phase detector
   a. introduced multiplier phase detector

   o pick up with discussion of its characteristics

Aside: Last day I gave a qualitative explanation of how a type 2 PLL works
   - Someone asked how it decreases in frequency, given that the nominal
     P.D. output is zero, and any pulses increase the frequency.
   - My answer wasn’t very clear, here is a clarification:

   - For the phase detector I was assuming (edge-triggered change in the
     duty cycle for output voltage), in the locked condition the nominal
     offset between \( \Phi_{in} \) and \( \Phi_{out} \) is 0. Red.
   - The output nominally has a 50% duty cycle, to put the avg output in the middle of the
     power rails.
   - If the freq. needs to be increased, the duty cycle is increased (ie. to 60%)
     for a time, then settles back to 50%. When lock is reacquired.
   - If the freq. needs to be decreased, the dut cycle is decreased (ie. to 40%)
     for a time, then it settles back to 50% when lock is reacquired.

Important point: The absolute phase offset between \( \Phi_{in} \) and \( \Phi_{out} \) is not
   necessarily zero for a type 2 PLL (it will depend on the type
   of phase detector employed), but it remains at this constant
   offset for all frequencies of operation, regardless of the
   frequency slope encountered.
- Redraw the previous example in a more accurate manner:

- Time domain signal wave forms:
  - increase input freq.
  - decrease input freq.
  - not accurately drawn!
  - back to 50.

- Hopefully that clears up any confusion.

- Now resume with the multiplier phase detector...

- **Multiplier Phase Detector**

- Vcc

- Check any analog I.C. design text for a more detailed description of the operation.
  - Don't worry too much about the details; you will not be tested on that explicitly, you will only need to know them if you decide to use it in the project.
  - For us, the important thing is that the output is a multiplication of the input signals.
  - Any mixer or non-linearity will work as a phase detector of this type.

- Continue with notes from previous lecture...
  - (These are the last ones that will be on graph paper)
- I will assume that everyone has seen this circuit before, and is familiar with how it operates.

- For small input signals (say less than 25 mV), the output voltage will be a multiplication of the inputs at A and B.

Let \( A(t) = A \cdot \cos(w_1 t + \phi_1) \) and \( B(t) = B \cdot \cos(w_2 t + \phi_2) \).

At output: \( V_{\text{out}}(t) = \alpha A \cos(w_1 t) B \cos(w_2 t + \phi_2) \)

\[ = \frac{\alpha \cdot A \cdot B \cdot \cos \left[ \left( w_1 + w_2 \right) t \right] + \alpha \cdot A \cdot B \cdot \cos \left[ \left( w_1 - w_2 \right) t - \phi_2 \right]}{2} \] \[ \square \]

\( \alpha \) - twice input frequency, filtered out by the loop filter.

- If PLL is locked, \( \phi_1 = \phi_2 \), and the output voltage is:

\[ V_{\text{out}}(t) = \frac{\alpha \cdot A \cdot B}{2} \cdot \cos(\phi_2) \]

Plot phase detector characteristics:

![Phase Detector Characteristic Graph]

Observations:
1) For \( w_1 \neq w_2 \) from \( \square \), we see that the average output of the phase detector is zero.

Q: How does the PLL acquire lock?
- We will solve this mystery when we discuss acquisition after phase detection.

2) Behavior is not linear, but when the PLL is locked, for large loop gains (or for Type 2 PLL), \( \Delta \phi \) will be close to \( \pm \pi/2 \) (or \( -\pi/2 \) depending on the error loop component), and we can approximate:

\[ V_{\text{out}}(t) \approx \frac{\alpha \cdot A \cdot B}{2} \cdot \left( 1 - \Delta \phi \right) \]

3) Input amplitude changes the phase detector gain (\( K_{\text{pp}} \)) and therefore alters the loop dynamics (undesirable) and the tracking range.
4) This type of phase detector performs well in the presence of a noisy input signal, but less so compared to other phase detectors we will consider (such as a multiplication range). It is not recommended for the project, since the source will be fairly "clean," assumed to come from a crystal oscillator.

Now, consider what happens if the amplitude of the input signals, \( A(t) \) and \( B(t) \), are much greater than \( kT/2 \).
- All the differential pairs will experience full swing, and the phase detector will behave like an XOR gate.

<table>
<thead>
<tr>
<th>( A(t) )</th>
<th>( B(t) )</th>
<th>( V_{out}(t) )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Plot the signal in the time domain: A

B

Nominal value of \( \delta \phi = \pi/2 \):

\( V_{out} \)

Introduce an initial phase offset:
- Note, average value of \( V_{out} \) has increased.

Plot output characteristics for equal frequencies:

- Similar to the multiplier, with monotonous characteristics from \( \delta \phi = -\pi/2 \) to \( \pi/2 \), but the operation stays linear over the entire range.
- This is good, it means loop dynamics will not change as \( \delta \phi \) changes.
Observations:
1) Phase error range is the same as for the multiplier, but the
more linear behavior results in increased tolerance range, due
to high Vout at extremes.

2) Like multiplier, average output for unequal frequencies is zero
(no frequency detection)
3) Input amplitude does not affect the behavior due to "digital"
operation (as long as it is sufficiently large)
4) Output is at twice the frequency of the input signal (thus
makes it easier to filter out the ripple)
5) Consider the effect of a change in duty cycle for one of
the signals:

\[ A \]
\[ \square \square \square \square \square \square \]
\[ \text{\text{B}} \]
\[ \square \square \square \square \square \square \]
\[ \text{Vout} \]
\[ \square \square \square \square \square \square \]
\[ \rightarrow \text{time} \]

This is the same phase offset \( \Delta \phi = \pi/2 \) as was illustrated
previously, but observe now that Vout will be lower
(stressed in text)

Thus, changing the duty cycle will change the output,
and this change the phase error in the locked
condition. This is undesirable

- We would like to eliminate the dependence on the duty cycle of the
inputs, to do this we can move to an edge-triggered design

3) R-S latch (also referred to as a 2-state phase detector)

A \rightarrow S \rightarrow Q \rightarrow \text{Latch} \rightarrow \text{Vout} \[ B \rightarrow R \rightarrow \text{Q} \rightarrow \text{Latch} \]

- Rising edge on A sets the output to "1"
- Rising edge on B resets the output to "0"

This is the phase detector we have been
assuming in our qualitative explanations of

Draw corresponding waveforms:

A \[ \square \square \square \square \square \square \square \square \square \square \square \square \]
B \[ \square \square \square \square \square \square \square \square \square \square \square \square \]
\[ \text{Vout} \]
\[ \square \square \square \square \square \square \square \square \square \square \square \square \]

- As input shift relative to each other, the
duty cycle (average value) of the output
will change
Plot the output characteristics for equal frequencies:

\[ V_{\text{out}} \] vs. \[ \Delta \phi \]

Compare to the XOR (assume same \( K_{\text{pp}} \)):

\[ V_{\text{out}} \] vs. \[ \Delta \phi \]

Observations:

1. The average output does not depend on the duty cycle (as desired).
2. Average output for unequal input frequencies is still zero.
3. Output is at the same frequency as the inputs, which makes it more difficult to remove ripple with the loop filter.
4. Comparing to the output characteristics of the XOR:
   - Slope is sawtooth instead of triangular
   - Linear range is centered around \( \pi \) instead of \( \pi/2 \)
   - Linear range is increased to \( 2\pi \) (from \( \pi \) for XOR), so for equal \( K_{\text{pp}} \), the RS-latch will have an extended tracking range.
5. This circuit will generate a non-zero dc output if one input frequency is an integer multiple of the other.

---

This could lead to false-locking, depending on the frequency range covered by the VCO.

There is one more very important type of phase detector, called a tri-state phase detector (or phase/frequency detector), but before we cover that we will discuss the acquisition process.

**Acquisition**

In examining PLL operation, there are three different ranges that are considered:

1. **Tracking Range (hold range):** This is what we discussed previously, where the input frequency is varied very slowly, so that the output frequency fails to follow only when it encounters a non-monotonicity in the P.D., L.P.F., or V.C.O. characteristics. This is the longest of the three ranges.
(2) Lock-in range: This is the behavior that we have assumed during our qualitative discussion of PLL operation for a frequency step. This is the range within which the PLL locks without any "cycle-slipping." Cycle-slipping occurs when the phase detector moves out of its linear range of operation due to the phase error becoming too large.

Illustration:

- Assume at \( t=0 \) the input freq. is changed.
- With each successive cycle, the phase error will increase (denoted by 1, 2, 3, etc. on plot).
- Size of phase error increment will be determined by the size of the frequency step.
- If frequency step is small enough, the loop response is fast enough, the feedback can increase the output frequency and bring back the phase error before it encounters the PLL non-linearity.

- If the frequency step exceeds the lock-in range, the phase error exceeds \( \Phi_{MAX} \) in the diagram and a "cycle-slip" occurs.
- This is referred to as the PLL losing lock, and lock must be reacquired through the "pull-in" process.
- This is the smallest of the three ranges.

(3) Pull-in range (acquisition range, capture range): This is what happens when the PLL cycle-slips before locking, as on a large frequency step, or likely upon power-up.
- As we will see, this is smaller than the hold range, although for a Type 2 PLL with a simple integration they would be the same.
- This can be a very slow process.

Summary of the three ranges:

- Fast locking
- Slow locking
- Hold range
- Pull-in range

Frequency steps in this range will never acquire lock.
Now let's examine the pull-in process.

For these analyses we will assume a multiplier P.D.

It can also be done with other types of phase detectors but most of the analyses in textbooks & literature is done for this P.D. and the values derived for this P.D. are a conservative estimate for other types of phase detectors (which will have improved pull-in characteristics).

We saw in our phase detector discussion that for unequal input frequencies, they have an average output of zero.

- During pull-in the input frequencies will be different, so how does the loop acquire lock?

To gain an intuitive understanding of the process, we will first examine it qualitatively in both the time & frequency domain, and then examine it quantitatively.

**Freq-domain behavior**

**Input**

![Diagram](image)

- Initial mixing operation produces a freq. component at \( \omega_n \) and one at \( 2\omega_n \). Assume fully attenuated by the loop filter.

- This signal (the "beat frequency") is applied to the VCO and modulated by an output frequency:

\[
V_{out}(t) = A \cos[ \omega_{in} t + K \alpha A \sin(\omega t) dt]
\]

\[
= A \cos[ \omega_{in} t + K \alpha A \sin(\omega t) ]
\]

\[
\approx A \sin(\omega_{in}) - K \alpha A \sin(\omega_{in}) \sin(\omega t)
\]

- This creates the spectrum shown in (a).

- Note the sidebands, this is the same process whereby ripple on the VCO control voltage due to inadequate filtering of the phase detector output by the LPF creates spurs.

- But in this case, as we will see, the spurs are a good thing.