Administrative Stuff:
1. Assignment #5 or Project #2 due today
2. Return Assignment #4
3. Final project assigned today
   - updated online project description
     - only need to implement the prescaler (mini div by 2)
     - can just do straight div by 2 and sacrifice lower reference frequency
     - can use dual-modulus divider if too costly a divider or choose a new one
     - added new Verilog divider to website with reset input for use as a simple counter
     - finished phase noise document, a website along with Matlab code.
     - Updated project description (phase noise affects changed)
   - due in 2 weeks, in final class or Thursday
   - don't want to extend it, so that you can study for the final over the weekend.
4. Final assignment will come out next week.
5. What to cover for final classes:
   - Today: PLL noise & Operations
   - Tues. Feb. 28: Freq. Synthesis
   - Thurs. Mar. 2: ?
   - Thurs. Mar. 7: ?
   - Thurs. Mar. 9: Review

Options:
1. Clock & Phase Recovery
2. Indirect modulation with PLL
3. PLL simulation issues
4. Direct digital synthesis
5. Digital PLL (low freq. or high freq. (TI paper))

→ Choose 2 of these topics
Recap from last class: 1. Phase noise in PLLs
   - general considerations
   - phase noise due to the reference
   - phase noise due to the VCO.

2. Professor Otis' research

→ Pick up with discussion of phase noise at PLL output due to other loop components,
   but first...

Notes on Phase Noise: 1. Due to assumptions made in the treatment of phase noise,
   there are theoretical contradictions encountered in the
   conventional analysis.
   - One example is that most phase noise components are
     non-stationary, so the rigorous definition of a P.S.D
     does not even exist.
   - Despite this shaky theoretical foundation, the result of these
     approximations is consistent with widely observed real-world
     behavior, so they remain useful for design.
   - For an in-depth discussion of PLL phase noise considerations,
     see Ch. 7 in [Phase-Lock Techniques, F.M. Gardner].

2. Regarding the apparent conflict between the assumption of
   white phase noise in deriving the noise-bandwidth of a
   PLL and the reality of a 1/f component for a real
   reference source:
   - PLL noise bandwidth is used in the context of PLLs
     with noisy input signals (i.e., PLLs used as filters,
     or for freq. demodulation) where the approximation of
     white noise is reasonable.
   - It would not be used with a freq. stable PLL with a
     XO reference input where 1/f noise is a dominant source.
   - It is just an assumption of a special case that
     greatly simplifies the analysis of noise at the PLL input.
   - For any signal with a 1/f noise component, the
     total integrated phase noise does not converge, as
     it goes to infinity as f→0, so this is not a
     relevant consideration.
   - For frequency synthesizers (as we will see when we discuss
     them), performance is usually specified by the phase noise
     at specific freq. offsets rather than the total
     integrated phase noise.
\[ \Phi_{in} \xrightarrow{+} [\text{K}_{PD}] \xrightarrow{F(s)} \xrightarrow{\text{K}_{VCO}} \xrightarrow{+} \Phi_{out} \]

\[ \Phi_{in} \xrightarrow{+} [\text{K}_{PD}] \xrightarrow{F(s)} \xrightarrow{\text{K}_{VCO}} \xrightarrow{+} \Phi_{out} \]

- Calculate the transfer function from the VCO phase noise to the output.

We find that:

\[ \frac{\Phi_{out}(s)}{\Phi_{in}(s)} = \frac{E(s)}{1 - H(s)} = \frac{N \cdot s}{N \cdot s + K_{PP} \cdot F(s) \cdot K_{VCO}} \]

- This is a high-pass function, with poles determined by poles of \( H(s) \).

  - Low frequency gain is zero (zero at DC).

  - High frequency gain is unity (no multiplication by \( N \) as for the reference noise).

So, phase-noise spectrum at the output due to the VCO phase noise is:

\[ S_{\Phi_{B}}(f) = |E(f)|^2 \cdot S_{\Phi_{in}}(f) \]

- So, to minimize phase noise at the output due to the VCO, we should minimize the loop BW.

Clearly, this conflicts with the requirement for the reference noise, so based on their relative levels, we must choose an optimum bandwidth for the loop (to be discussed subsequently).

3. Other Loop Components

- Typically, the noise from the reference \( \Phi_{ref} \) dominates the phase noise at the PLL output, but all components can contribute noise, so we will enumerate their effects for completeness.

- Redraw the model:

\[ \Phi_{in} \xrightarrow{+} [\text{K}_{PD}] \xrightarrow{F(s)} \xrightarrow{\text{K}_{VCO}} \xrightarrow{+} \Phi_{out} \]

\[ \Phi_{in} \xrightarrow{+} [\text{K}_{PD}] \xrightarrow{F(s)} \xrightarrow{\text{K}_{VCO}} \xrightarrow{+} \Phi_{out} \]

\[ \frac{1}{N} \]

(a) \( \Phi_{n, \text{div}} \)

(b) \( \Phi_{n, PD} \)

(c) \( \Phi_{n, LF} \)
(a) Divider - The divider noise experiences the same transfer function as the reference noise \( H(f) \).
- The sampling nature of the digital divider results in aliasing of the input noise to lower frequencies. References to examine this are provided in [Phase-Lock Techniques, Gardner].

(b) Phase Detector - T.F. for phase detector noise is:

\[
\frac{E(s)}{N \cdot s + Kpp \cdot F(s) \cdot Kvo \cdot Kpd} = H(s) = \frac{E(s) \cdot Kvo}{N \cdot s + Kpp \cdot F(s) \cdot Kvo \cdot Kpd} \cdot s
\]
- Low-pass filtered and multiplied by \( N \), as for reference noise.
- Higher \( Kpp \) leads to lower output phase noise contribution from the phase detector.

(c) Loop Filter - T.F. for loop filter noise is:

\[
\frac{Kvo \cdot N}{N \cdot s + Kpp \cdot F(s) \cdot Kvo \cdot Kpd \cdot F(s)} = H(s) = \frac{E(s) \cdot Kvo}{N \cdot s + Kpp \cdot F(s) \cdot Kvo \cdot Kpd \cdot F(s)} \cdot s
\]
- Small \( VCO \) gain will minimize the effects of loop-filter noise.
- If PLL i) type 2 or higher, this noise will be low-pass filtered.

\[ \text{VCO output noise examples (insert on previous page)} \]

\[ \text{Optimum loop bandwidth} \]

As mentioned, assuming that the reference of VCO phase noise is the dominant contributor to the output phase noise, some optimal loop B.W. can be chosen to minimize the total output phase noise.
If the PLL noise is dominated by the noise from the reference and VLO, it can be shown (but not by me) that the optimum PLL B.W. (from a noise perspective) is close to the frequency crossover of the VLO phase noise spectrum and the N-multiplied phase noise spectrum of the reference.

→ This rule does not account for noise of other components, they may force some adjustment of the band-width.
→ A crossover frequency may not exist, or in the case for modern freq. synthesizers with noisy integrated VLO, this rule may call for a higher B.W. then is possible (due to stability limitations).

Intuitive view of previous results:

→ Reference noise: Noise on the input at low frequencies will be tracked at the output, thus the lowpass T.F.
→ VLO noise: For low freq. VLO noise, the loop will adjust the control voltage in the other direction to cancel out the noise, but for high freq. noise, the loop cannot respond quickly enough, thus the highpass T.F.

Phase Noise Analysis for the Project

→ To analyze the noise performance of non-linear RF circuits, we use PSK (Periodic Steady State) Analysis (explain)
Running this on the complete PLL would be too slow, so we run it for individual components and then use Matlab to combine their effects at the output after filtering by the appropriate transfer functions.

- Get phase noise spectrum for each of the dotted blocks, $S_{\phi}(f)$ and multiply each by the squared magnitude of the appropriate T.F., then sum them at the output for the total phase noise power (Matlab code for this will be supplied).

1. Oscillator - use phase noise spectrum supplied by XO manufacturer (already in the Matlab code)
2. Phase Detector, Charge pump (if using), Loop Filter - use Cadence PSS simulation to obtain noise profile (amplitude noise), export data to Matlab
3. VCO - use Cadence PSS simulation to obtain phase noise profile, export to Matlab
4. Divider - use Cadence PSS simulation to obtain phase noise profile, export to Matlab
A radio transceiver needs a stable LO (local oscillator) signal that can be used for up/down conversion of the baseband signal for transmission/reception.

General receiver architecture:

- For a given standard, the frequency spectrum in some band will be partitioned into a number of channels, each having the same bandwidth.
- The band-select filter selects this entire band of frequencies.
- Each channel can contain information, so the received spectrum after the antenna can look like this:

```
\[ \text{channel select filter} \]
```

The mixer uses the LO signal to downconvert the selected channel to a fixed frequency (assume 0 for an example), where the channel select filter eliminates other content.

```
\[ \text{LO signal} \]
```

At different times, the transceiver must transmit and receive on different channels, so the LO signal must be variable throughout the entire frequency band, in increments of the channel frequency.

- This is why a PLL is used for the LO.
- An accurate crystal oscillator (usually within 10 ppm) is supplied as the reference frequency, and a divider in the feedback path is used to multiply this up to the appropriate LO frequency.
1. Phase Noise

Consider the ideal case of demodulating one sinusoidal signal with another:

\[ \text{desired signal} \rightarrow \text{LO output} \]

\[ W_0 \rightarrow W \]

\[ \Rightarrow \]

\[ \text{note that the desired signal has not been affected by the interference.} \]

Now consider the case where the LO has phase noise:

\[ \text{interferer} \]

\[ \text{desired signal with phase noise} \rightarrow \text{LO with phase noise} \]

\[ \Rightarrow \]

\[ \text{how the desired signal has been corrupted by neighboring interferers.} \]

\[ \Rightarrow \]

So, we would like phase noise to be as low as possible.

Phase noise requirements for a PLL used as a frequency synthesizer for a particular communication standard from the required SNR and the allowable levels of nearby interferers.

2. Spur

Now consider demodulation where there is a strong signal being received in an adjacent channel, and the LO signal has a spur (could be due to reference feed-through, as discussed earlier) at a frequency offset of the channel bandwidth from the LO.

\[ \text{REF input: weak desired signal} \rightarrow \text{strong interferer in adjacent channel} \]

\[ \text{LO signal:} \]

\[ \Rightarrow \text{LO} \]

\[ \text{spur} \]

\[ W_0 - W_s = W_0 - W_{\text{int}} \]

\[ \text{Mixer output:} \]

\[ \text{interferer now overlaps the desired channel, and cannot be filtered out.} \]
→ for a given standard, allowable spur levels at different frequency offsets can also be calculated based on the specified SNR of maximum adjacent channel power levels.  

→ So, we want to minimize spur levels.


→ When a cellular phone user moves into a new cell, it may be necessary for them to switch the channel they are transmitting/receiving on according to what channels are open in the new cell.

→ This requires that the LO be switched to a new frequency.

→ To avoid causing interference to other users, the LO must settle to within some specified margin of the final frequency (otherwise it could be transmitting in the bandwidth of an adjacent channel).

→ To avoid disruption of service, a standard will specify some maximum settling time for the frequency synthesizer in moving to the new channel.

4. Power

→ When used in a handset, low power consumption leads to longer battery life, so power consumption of all components (including the PLL) should be minimized.

5. Area

→ Smaller chip area leads to cheaper manufacturing costs, so area of all components (including the PLL) should be minimized.

→ Coincidentally, these are the 5 criteria that you are optimising your projects for.

→ Now let’s examine different PLL architectures for frequency synthesis, and see how they allow us to meet the criteria specified above.

1. Integer-N PLLs

   \[
   \text{Out} \xrightarrow{\text{Phase}} \xrightarrow{\text{Modulator}} \xrightarrow{\text{Filter}} \xrightarrow{\text{VCO}} \xrightarrow{\text{Out}} \xrightarrow{\text{Feed}}
   \]

   \[
   \text{Div} \xrightarrow{\text{Div}} \xrightarrow{\frac{1}{N}}
   \]

→ This is the architecture we have been implicitly assuming up until this point.

→ Operation: the negative feedback of the loop forces \( \text{Out} \) and \( \text{Div} \) to have some constant offset.

→ i.e. \( \text{Out} = \text{Div} \)