1. Your expression should include only real resistances (R_{G1}, R_{G2}, R_1, R_2, R_3, R_4, R_L, or a subset of these) and possibly β, r_e1 or r_{π1}, and r_e2 or r_{π2}. (Assume both BJT transistors have the same β.)

(a) Assume the transistors below have a finite β and an infinite Early voltage. Ignore λ. Write an expression for the input resistance \( R_{in} \) in the circuit shown below.
(b) Assume that \( V_A=20V \) for Q2 while all other transistors have infinite Early voltage. Write an expression for the output resistance \( R_{out} \) in the circuit shown below including \( r_o2 \).

![Circuit Diagram]

2. (a) Circle the answer that is the most appropriate:

(i) Common-mode rejection ratio: 0.05 100 0.01
(ii) Common-mode gain: 0.05 100 0.01

(b) Answer True or False to the following questions:

(i) Looking at the circuit on the right, if \( R_e \) is increased, the gain increases.
(ii) The input offset voltage for a BJT differential amplifier is directly related to a change in input signal.
(iii) Input bias current in a MOS differential amplifier is due to the difference in (W/L) of the transistors.
(iv) The input offset voltage for a MOS differential amplifier increases with an increase in \( I_{bias} \).
3. An uncompleted circuit consisting of two differential pairs is shown below. We wish to create a biasing network so that the **NMOS** differential pair has a differential gain equal to 100V/V, and the **pnp** differential pair transistors each have a $g_m$ of 15.36mA/V. Assume that $\beta$ is very large, $k_n'(W/L) = 1.2mA/V^2$, $|V_{BE}| = 0.7 V$, $|V_A| = 40V$, (threshold voltage) $V_t = 0.5V$, and (thermal voltage) $V_T = 25 mV$ for this entire problem. Neglect the Early Effect for the BJT transistors.

(a) State the required dc bias voltage (VGS) needed for the NMOS differential pair to work correctly.

(b) What value of $I_1$ is required?

(c) What value of $I_2$ is required?

(d) Now, on the schematic below, draw a current mirror biasing network to provide the required dc currents. You may use no more than 3 nmos transistors, 3 pnp transistors, and one resistor of any value. Assume all transistors of the same type are identical in size. You may only use $V_{DD} = +5$ V power supply.

(Don’t worry about connecting anything to the inputs or outputs of the differential pairs; we’re only concerned with the biasing network in this problem. Assume that the MOSFET’s are biased to a saturation region. Don’t worry about the resistor values in the collector of the BJT.)
4. An active-loaded MOS differential amplifier is shown below. The transistors are specified as follows: 
\((W/L)_n=10, (W/L)_p=20, \ k_n'=2k_p'=200\mu A/V^2, |V_A|=100V, V_{DD}=10V, \text{ and } |V_I|=0.7V.\) Design the circuit below so that \(A_d= 60V/V.\)
(a) State the value needed for \(I\) and \(R.\)
(b) Determine CMRR.
(c) What is the voltage range for \(V_{CM}.\) (minimum and maximum values for the input gates)

5. Consider the basic bipolar differential circuit (shown to the right) in which the transistors have \(V_{DD}=10V, \beta=100\) and \(V_A=100V,\) and \(R_c=20k\Omega.\) Find:
(a) The value of \(R_E.\)
(b) the differential gain \((V_{o2}-V_{o1})/V_{id}\)
(b) the differential input resistance
(c) the common-mode rejection ratio when the resistors in the collector are 2% accurate.
Design the circuit below to achieve a DC bias of $I_E=1\text{mA}$. Use $\beta=100$ and $V_A=50\text{V}$ for all transistors. Assume $V_{BE}=0.7\text{V}$.

6. (a) State the value of $I_{REF}$.
   (b) Derive an expression for $R_{in}$, $R_{out}$, and $A_M$(midband gain)

7. (a) Select values for $C_E$ and $C_C$ to place the 2 break frequencies at 10Hz and 100Hz.
   (b) Calculate $f_H$ when $C_\pi=16\text{pF}$, $C_\mu=0.3\text{pF}$, and ignore $r_x$. (Ignore the frequency effect due to the current source)
8. Use $g_m=1\text{mA/V}$, $C_{gs}=2\text{pF}$, and $C_{gd}=0.4\text{pF}$. Find: (a) $f_L$, (b) $A_m$(midband gain), (c) $f_H$.

9. Assume all transistors are matched. The transistors are specified as follows: $(W/L)_n=10$, $(W/L)_p=20$, $k_n'=2k_p'=200\mu\text{A/V}^2$, $|V_A|=100\text{V}$, and $|V_t|=0.7\text{V}$.
(a) Determine the overdrive voltage.
(b) What is the allowable voltage range at the output (drain of Q2).
10. Use $\beta=100$ and $V_A=50\,\text{V}$ for all transistors. Assume $V_{\text{BE}}=0.7\,\text{V}$ and $V_{\text{BC(on)}}=0.4\,\text{V}$. Find
(a) $R_{\text{in}}$
(b) $R_{\text{out}}$
(c) $V_{o1}/v_{\text{in}}$
(d) Approximate value of $V_{o2}/v_{\text{in}}$