SIMMAT
A Metastability Analysis Tool

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Outline

- Introduction and Motivation
- Synchronizer behaviors
- Metastability analysis using SIMMAT
- Video animation of SIMMAT
- Conclusion
Introduction

- Multiple independent clock domains on processor chips
- Synchronizers employed to ensure reliable data transfers between clock domains
Motivation

Modern processors in sub-micron processes:
- multiple clock domains, 100’s of synchronizers
- frequencies > 3 GHz
- transistors have lower gain
- severe layout parasitic capacitance

Metastability characteristics:
- both large-swing and small-swing signal behavior
- possible to measure, but unable to use conventional simulation due to numerical stability and precision limits
- possible to estimate from circuit equations, but non-trivial to analyze multi-stage synchronizers
SIMMAT

A Metastability Analysis Tool

Enables estimation of metastability characteristics during circuit design rather than after fabrication.

Built on top of conventional simulators, such as Hspice and SmartSpice.

Used for:
- characterizing deep metastability behavior
- comparing synchronizer circuits and layouts
- evaluating effects of adding scan test circuits
- exploring state machine failure resulting from prolonged metastability
Increased Clk to Q Delay

Synchronizer circuit samples input data and decides if data are HI or LO. Occasionally the data are sampled when changing and the decision response is delayed – can cause circuit malfunction.
Synchronizer Analysis Waveforms

![Diagram of master and slave latches with simulation waveforms](image-url)

- **clk**: Clock input
- **d**: Data input
- **q**: Output

Simulation waveforms show the voltage levels over time (ns) for the inputs and outputs.
Synchronizer Characteristics

Simulation analysis:
Time Window size, \( \Delta \text{tin}(T_s) \), for Settling Time values, \( T_s \)

- \( T_{\text{w(nom)}} < \text{setup + hold} \)
- MTBF increases exponentially with \( T_s \)

MTBF = \[ \frac{\exp \left( \frac{T_s}{\tau} \right)}{T_w \times f_c \times f_d} = \frac{1}{\Delta \text{tin}(T_s) \times f_c \times f_d} \]

\[ \text{MTBF} = T_w \times f_c \times f_d \]

\[ \Delta \text{tin}(T_s) \times f_c \times f_d \]

Graph:
- Time Window, \( \Delta \text{tin}(T_s) \) seconds (log scale)
- \( T_w \)
- \( T_{\text{w(nom)}} < \text{setup + hold} \)
- \( \tau = -1/\text{slope} \)
- GOOD
- BAD

[Graph showing the relationship between settling time and time window with labeled axes and points.]
Operating Point

Time Window, $\Delta \text{t}_{\text{in}}(T_s)$ seconds (log scale)

$\text{Tw}$

$\text{Tw(nom)}$

$-30$

$-60$

$\tau = -1/\text{slope}$

$\text{clk}$

$\text{Ts(nom)}$ (clk $\rightarrow$ q)

Settling Time, $T_s$

Receive clock

Synchronizer

Logic
Metastability Analysis Results

The diagram shows the settling time, $T_s$, in a time window, $\Delta t_{\text{in}}(T_s)$, measured in logarithmic seconds ($\log_{10}$ seconds). The graph compares different metastability situations:

- **1 FF stage**
- **2 FF stages**
- **3 FF stages**

Each line represents a different number of FF stages, with the 3 FF stages showing the longest settling time, followed by 2 FF stages and then 1 FF stage.
Example MTBF Calculations:

A signal crossing into a 3 GHz clock domain from a 2 GHz clock domain, where the signal changes on average at 0.25 * 2 GHz

\( fc = 3 \text{ GHz}, \quad fd = 0.25 \times 2 \text{ GHz}, \quad \text{at } Ts = \text{clock-to-q delay + slack time:} \)

- 1 FF stage: \( \Delta t_{in}(Ts) = 10^{-17} \) seconds
  
  \[
  \text{MTBF} = \frac{1}{((10^{(-17 + 18)}) \times 3 \times 0.25 \times 2)} = 60 \text{ msec}
  \]

- 2 FF stages: \( \Delta t_{in}(Ts) = 10^{-26} \) seconds
  
  \[
  \text{MTBF} = \frac{1}{((10^{(-26 + 18)}) \times 3 \times 0.25 \times 2)} = 2 \text{ years}
  \]

- 3 FF stages: \( \Delta t_{in}(Ts) = 10^{-37} \) seconds
  
  \[
  \text{MTBF} = \frac{1}{((10^{(-35 + 18)}) \times 3 \times 0.25 \times 2)} = 2e+9 \text{ years}
  \]
State Machine Failure

State change from "State A" to "State B" enabled by control signal output from a synchronizer

State change involves multiple bit transitions

Delayed synchronizer response can produce an incomplete state change, ending in failure states "State F1" or "State F2"

Can use SIMMAT to analyze the failure probability
Video Animation

Simulation Waveforms

Metastability Characteristics

Increased clock-to-q delay
Conclusion

SIMMAT:
- Enables analysis of multi-stage synchronizers in deep metastability
- Characterizes synchronizer circuits \(\rightarrow\) MTBF
- Facilitates design of new circuits
- Explores bi-modal circuit behavior
Extra Slides
Long Time-constant Output

Output amplifier has switching voltage very close to metastable voltage of slave latch
Multiple Output Transitions

Master and slave latches have slightly different metastable voltages while the switching voltage of the output amplifier lies between these two voltages.
Metastability During Initialization

Clock-phase generator for source-synchronous communication

A self-resetting gate that during initialization can exhibit metastability that persists for multiple clock cycles