Basic Phase-Locked Loop

Objectives

The objective of this lab is to learn the basic concepts of operation of phase-locked loops (PLL). Experiments cover the measurement of the gain of a voltage-controlled oscillator and the construction of a PLL with a first-order filter. PLL properties such as capture range, hold range, transient response, and steady-state ripple are measured, and correlated with analysis results.

Introduction

A *phase-locked loop* (PLL) is a device in which a periodic signal is generated and its phase is locked to the phase of an incoming signal. Phase-locked loops are used for the demodulation of frequency-modulated signals, for frequency synthesis, and for other applications. The principles of operation of phase-locked loops are discussed in the course notes. Familiarity with the relevant equations is assumed.

Pre-lab

The pre-lab consists in computing the gain of phase detector I of the phase-locked loop chip used in the lab. In the notes, a phase detector based on a multiplier was discussed. Here, the phase detector is a logical XOR operator. The two signals entering the phase detector are assumed to be square waves with logic levels at 0 and V_s (in Volts). The output of the XOR phase detector also varies between 0 and V_s.

Assuming that the two input signals have the same frequency, sketch the output signal when the inputs signals have a phase difference of 0°, 90°, and 180°. Then, plot the *average value* of the output signal for a phase difference ranging from $-180°$ to 180°. Show that, within the range $0 \to 180°$, the average value of the output of the phase detector satisfies

$$\phi = k_{pd} \left(\theta - \theta_{vco} \right) \tag{1}$$

Give the value of k_{pd} in V/rad when $V_s = 12V$. The voltage-controlled oscillator (VCO) of the PLL chip is biased so that the center frequency is produced when the applied voltage is $V_s/2$. What phase difference produces this output of the phase detector? The phase difference is the one that will be observed when the PLL is locked and there is no frequency error.

Laboratory

The laboratory covers two main tasks: measuring the gain of the VCO and designing a PLL with first-order filter. Parts of this lab and of the next lab use the same circuits. Therefore, review the schematic of the next circuit to be built before disassembling the current one. There is a low temperature coefficient capacitor (3900pF) that is needed in the lab. It is necessary to insure repeatability in the experiments. The small epoxy coated, shiny, smooth, light brown capacitors with a 392 printed on them should work fine. Do not use the bigger, dull, brown rectangular or disc-shaped capacitors. The 39 stands for 39 and the 2 means to add two zeros to get 3900pF.

Measuring k_{vco}

EQUIPMENT NEEDED (use a bench having the equipment, if available): oscilloscope, frequency counter, function generator, power supply, and a DMM.
EQUIPMENT TO BE CHECKED OUT: wire kit, two 10x probes, and a Wavetek function generator.
PARTS NEEDED: CD4046 CMOS PLL IC, 3900pF low temp. coef. capacitor, 2 resistors that will be determined in the lab, $0.1\mu F$ cap., $10k\Omega$ multi-turn POT (with "tweaker"), $10k\Omega$ and $1k\Omega$ resistors, proto-board and wires.

Begin by calibrating the 10x probes to your oscilloscope. If you are unsure of how to do this, check out the booklet titled "The XYZ's of Using An Oscilloscope," and read Chapter 8. The information is still useful even though the book is written for a different oscilloscope. If you are unsure where the probe adjustment is, check with your classmates, the TA, or the stockroom attendant. Then, set the power supply to 12 volts DC.

A WORD ABOUT STATIC
The PLL IC that you will be using is a CMOS part and is static sensitive. Following a few precautions will avoid zapping your IC. First, ground yourself to your circuit before inserting the IC or working on the circuit. Second, never assemble or change your circuit with the power applied. Third, connect signal and power sources ground lead first. Fourth, apply circuit power first, then signal sources. To change your circuit, remove signal sources first, then power. Last, disconnect signal and power sources ground lead.

Assemble the circuit shown in Fig. 1. The VCO frequency range will be from 30kHz to 50kHz. The datasheet for the CD4046 indicates that this range is achieved for R1=18$k\Omega$, R2=18$k\Omega$, and C=3900pF. Be sure to keep the $0.1\mu F$ capacitor as close to the PLL IC as possible without trimming the leads.
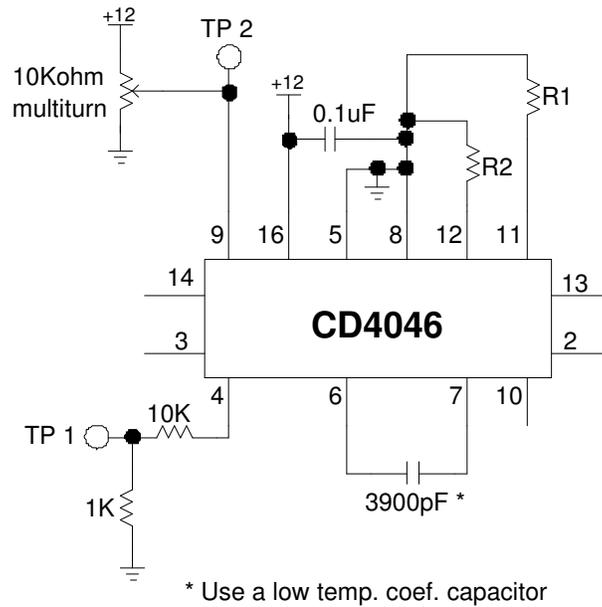
The significant pins of the PLL chip are:

Figure 1: Schematic used to measure the gain (k_{vco}) of the VCO

- pin 14: input #1 of the phase detector.
- pin 3: input #2 of the phase detector.
- pin 2: output of phase detector I.
- pin 4: VCO output.
- pin 9: VCO input.

AC COUPLING OR DC COUPLING?

Incorrect channel coupling can wreak havoc on measurements and cost you a lot of time. AC coupling places a high-pass filter in series with the probe to remove the DC component from the measurement. Use AC coupling if you are measuring high frequencies that have large DC offsets. However, AC coupling at low frequencies can lead to phase and amplitude errors. For accurate measurements below 300Hz, use DC coupling. It is best to use DC coupling whenever you can because it is so easy to forget that you are on AC coupling.

Having built the circuit, connect the DMM to TP 2 and the frequency counter to TP 1. Adjust the VCO control voltage with the $10k\Omega$ POT, and make a plot of frequency *vs.* voltage. Determine the range of control voltage that results in a linear VCO response and determine the gain of the VCO, or k_{vco} (in Hz/V), in that range. Deduce the value of the loop

gain, $k_{pll} = 2\pi k_{vco}k_{pd}$, using the value of k_{pd} determined in the pre-lab. Note that the transfer function from the VCO input to the output of the phase detector is then

$$P(s) = \frac{k_{pll}}{s} \tag{2}$$

and constitutes the "plant" to be controlled.

Basic PLL

In this section, you will build a PLL circuit with first-order loop filter and measure its characteristics. Considering the circuit shown in Fig. 2, show that the transfer function of the loop filter (which takes the role of the compensator) is

$$C(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{k_f}{s + a_f} \tag{3}$$

and give k_f and a_f as functions of Rf and Cf. Using the value of the gain k_{pll} determined in the previous section, determine the condition that Rf and Cf must satisfy so that the closed-loop poles have damping $\varsigma = 0.707$ (partial answer: $a_f^2 = 2k_{pll}k_f$). From the list below, find the correct combination of Rf and Cf:

a) $10k\Omega$ and 3300pF   e) $51k\Omega$ and 1000pF
b) $18k\Omega$ and 2200pF   f) $15k\Omega$ and 390pF
c) $15k\Omega$ and 4700pF   g) $22k\Omega$ and 470pF
d) $18k\Omega$ and 820pF   h) $120k\Omega$ and 4700pF

Verify your choice with the TA and build the circuit of Fig. 2. The main added parts from the previous circuit are Rf and Cf, but note the small changes. Apply circuit power, set the Wavetek to 40kHz, 8 volts p-p sinusoid, and connect it to the circuit. Observe the signal input on TP 3 and the VCO signal on TP 5. Trigger the scope on TP 3. Also, for your convenience, connect the frequency counter to the input signal TP 3. With this set-up, the two waveforms on the scope should appear "in sync." In other words, the VCO waveform should be stationary and at the same frequency as the input waveform (the PLL is locked). If not, double check your PLL circuit and the loop filter values.

Now, slowly decrease the input frequency. As you drop below 30kHz or so, you should notice that the VCO signal looses sync with the input signal. To explain what happened, set the input back to 40kHz and measure the voltage at TP 4 with the DMM (set to DC). TP 4 is the VCO control voltage input. It is the voltage that you measured when making the plot of VCO frequency *vs.* control voltage. Again, decrease the input frequency and observe the voltage on the DMM. Now, can you explain what happens when the input frequency drops below 30kHz? Compare to what happens when you adjust the input frequency above 50kHz. Between 30kHz and 50kHz, does the VCO frequency track the input frequency?
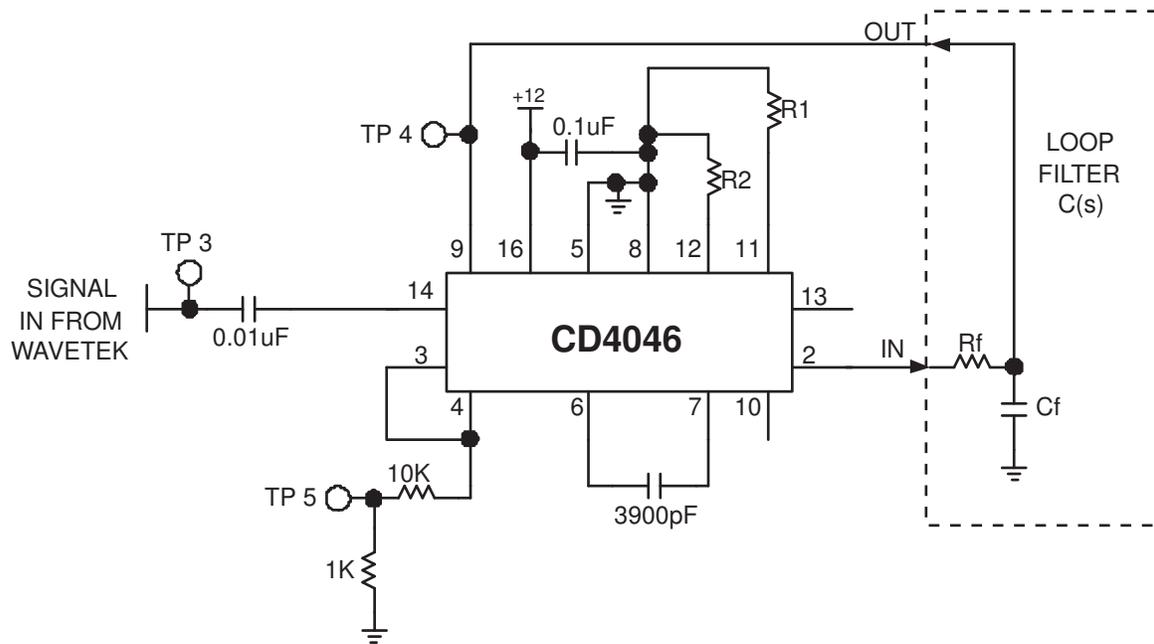
Figure 2: Schematic of a PLL with first-order filter

A QUICK REVIEW OF OSCILLOSCOPE PHASE MEASUREMENT
Measuring phase on the oscilloscope is quite easy. It is simply the measurement of the time between two points on two waveforms. The time measured is divided by the signal period and multiplied by 360 degree to give the phase difference. Specifically, set the scope to view two channels simultaneously. Set the trigger source to the channel you wish to be the reference channel. For this lab, the trigger should be set to the rising edge. Choose a point on the reference signal. Designate this point as the $t = 0$ point and position the point so that it crosses the center horizontal graticule. Find the same point on the second channel signal and position it vertically until it crosses the center horizontal graticule. Measure the time delay between the two points using the marks on the horizontal graticule and the horizontal time base. If the signal frequency is known, multiply the time measured by the frequency (equivalent to dividing by the cycle period), and then multiply by 360 to obtain the phase difference in degrees.

Measure the PLL's hold range and capture range. The hold range is the range of input frequencies for which the PLL maintains phase lock. The capture range is the range for which the PLL acquires phase lock. To measure the hold range, start the input frequency at a point where the PLL is phase-locked, then reduce the input frequency until the PLL looses lock. The

frequency is the lower edge of the hold range. The upper edge is obtained similarly by raising the input frequency. To measure the capture range, start the input frequency at a point where the PLL is not phase-locked, and raise the frequency until the PLL acquires phase lock. The frequency is the lower edge of the capture range. The upper edge is obtained by lowering the incoming frequency from a frequency above the capture range. The frequency counter should help in quickly determining the input frequency. If the frequency adjust knob is too coarse of an adjustment, try using the frequency vernier knob for fine adjustments. Next, make a plot of the input phase *vs.* input frequency over the range in which the PLL is locked (4 or 5 frequency points). Does the phase remain constant over the input frequency range? Can you explain the answer based upon the properties of phase-locked loops with first-order filters?

Next, set the input frequency to 40kHz and measure the VCO control voltage input (TP 4) with the scope. Is this control voltage a nice clean DC voltage? If not, how much ripple is present? What is the source of the ripple? Hint: remember the time constant of the loop filter, and use the scope to observe pin 2 on the PLL. In theory, the ripple could be decreased by lowering the bandwidth of the loop filter. However, the constants k_f and a_f cannot be set independently. To find out what would happen if the bandwidth of the RC filter was decreased, sketch the root-locus of the closed-loop poles as functions of the product Rf.Cf, and explain why increasing the time constant of the loop filter is not desirable.

Next, the Wavetek frequency will be modulated by a square wave to view the PLL step response. Set-up the extra generator (mounted in the workbench) for a frequency of 200Hz and a square wave output. With the output at minimum, connect the output to the VCG input of the Wavetek (lower left connector). Also, using the BNC "T", observe the bench generator output on one channel of the scope while observing TP 4 on the other channel. Trigger from the bench generator. Slowly increase the bench generator output. The square wave output is frequency-modulating the Wavetek output. If you adjust the bench generator output too high, the Wavetek output frequency will shift beyond the hold range of the PLL. With the Wavetek frequency knob still set to 40kHz, adjust the bench generator output level until TP 4 has a 5 volt p-p square wave. Describe the response of the VCO control voltage (TP 4) in terms of speed of response and overshoot.

This is the end of the basic PLL lab. Do not take apart your PLL circuitry. Most of it will be used in the advanced PLL lab.