1. Fill in the missing parts of the timing diagram below.

CLK

D

Q

2. Fix the truth tables in Figures 12.85 (p691) and 12.86 in the textbook so that they match Figure 12.87 on the Reset and Set lines.

<table>
<thead>
<tr>
<th>J</th>
<th>K</th>
<th>Q</th>
<th>\overline{Q}</th>
<th>Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
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<td></td>
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<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>Reset</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Set</td>
</tr>
<tr>
<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

These two lines:

3. Fill in the missing parts of the timing diagrams below.

a)

CLK

J

K

Q

b)

\overline{CLK}

J

K

\overline{PRE}

\overline{CLR}

Q
c) When the clock is enable and clock is input, the circuit is a two-bit counter with the clock as the input, $Q_1$ as the LSB of the output and $Q_2$ as the MSB.

e) What does the circuit of part c) do when it is enabled and there is a clock.

Answers

1. 

3.a) 

e) It's a two bit counter with the clock as the input, $Q_1$ as the LSB of the output and $Q_2$ as the MSB.