ECE/CS 5710: Digital VLSI Design

Credits and Contact Hours: 4.0 Credit Hours
15 weeks: Two 80-minute lectures per week
6 hours per week lab time for learning tools and developing chip design

Instructor’s Name: Ken Stevens

Text Book(s) and/or Required Material:
- E. Brunvand, *Digital VLSI Chip Design with Cadence and Synopsys CAD Tools*, Addison-Wesley, 2010

Catalog Description: Basic concepts of the design of digital CMOS integrated circuits. Course topics include static and dynamic properties of MOS circuits, composite layout of CMOS circuits, modeling of transistors for stimulation, and commonly encountered CMOS circuit structures. Students complete design, composite layout, and simulation of a simple integrated circuit using computer-aided design tools.

Prerequisites:
- C- or better in ECE/CS 3700: Fund. of Digital System Design; and
- Full major status in Electrical Engineering or Computer Engineering

Designation: Elective

Contribution of Course to Meeting the Requirements of ABET Criterion 5: Engineering sciences and engineering design

Specific Outcomes of Instruction:
In this class students will:
1. Learn how to drive Electronic Design Automation (EDA) Computer-Aided Design (CAD) tools;
2. Learn the physical mask design for transistors and how to create and characterize their own logic cell library; and
3. Using the cell library, design a complete integrated circuit architecture including power delivery and bonding pads.

Relationship of the Course to the Program Outcomes:
(a) An ability to apply knowledge of mathematics, science, and engineering. Students apply fundamental concepts of electronic circuits including resistance, capacitance and inductance models, current equations for transistors in three major operational modes, and develop and apply state machine models in Verilog to solve exam and design problems.
(b) An ability to design and conduct experiments, as well as to analyze and interpret data. During an initial set of laboratory assignments the students develop the layout for a set of combinational gates as well as a sequential flip-flop cell. These are evaluated for performance, power, area, and functional correctness. During the labs they are taught how to characterize the cells for inclusion in automated synthesis and place and route.

(c) An ability to design a system, component, or process to meet desired needs within realistic constraints such as economic, environmental, social, political, ethical, health and safety, manufacturability, and sustainability. The last third of the class is spent developing a significant integrated circuit design based on the cell library developed in the first part of the course. The design must meet performance, power, and area specifications for the design. Design rule verification and equivalence verification to a reference are performed to ensure manufacturability. Of the project. Some of the projects will be fabricated and the physical integrated circuit tested in the next semester.

(d) An ability to function on multidisciplinary teams. The projects are all performed with teams of three to five students.

(e) An ability to identify, formulate, and solve engineering problems. Engineering tradeoffs in the design of an integrated circuit design is taught and developed in the final chip design project.

(g) An ability to communicate effectively. The student will write a project proposal describing what they will develop, the specifications of the design, and a timeline for the development of their project. When the project is complete, they will give a presentation describing their engineering tasks and results as well as produce a final report on their design.

(k) An ability to use the techniques, skills, and modern engineering tools necessary for engineering practice. The first two thirds of the class are focused on teaching the students to use the EDA tools from Cadence and Synopsys. These tools are used for the specification, design, simulation, and validation of their engineering project, which includes the physical design and characterization of a cell library and a project that uses the cell library to develop and validate a significant project ready for manufacture.

**Topics Covered in the Course:**
- Basic transistor theory
- CMOS processes
- VLSI CAD tools
- Mask layout methods and design rules
- Circuit simulation and characterization
- Custom datapath design
- Design validation
- Full chip assembly
- Architecture and design of various key architectural function blocks