Thermal conductivity absolute-pressure sensors are widely used in vacuum systems. Their operation is based on the pressure dependence of the heat transfer from a suspended hot filament through a gas. The filament temperature and IV curve are dependent on the heat transfer and hence on the gas pressure. This mechanism has been studied thoroughly by V. Ubisch and others. Recently, microbridge resistor structures consisting of a resistive doubly-supported beam suspended above the substrate have been used to detect absolute gas pressure. The pressure-dependent heat transfer in these structures occurs across the gap between the beam and the substrate.

Figure 1 shows a schematic cross section of the microbridge designed for this chip. It consists of a n+- polysilicon beam coated with low-residual stress silicon nitride suspended over a 25μm-deep V-groove etched into the silicon substrate. The beams are typically 400 to 600μm long, 1μm thick, and 3μm wide. These structures are fabricated along with MOS devices on the same substrate using a 14-mask process. A 1μm-thick oxide passivation layer is deposited everywhere to protect the Al metal interconnect and MOS devices from the silicon etch used to form the V-groove. The passivation is then plasma-etched on the microbridge areas, and the V-groove is carved into the substrate with ethylenediamine-pyrocatechol-water anisotropic silicon etch. Figure 2 shows a SEM micrograph of the microbridge.

Figure 3a shows the organization on-chip of the microbridge sensor, constant-resistance bias circuit, and resistor-string 8b SAR A/D converter. The output of the chip is a robust digital signal representative of absolute pressure. All the circuits are implemented in a 4μm nMOS technology merged with the microbridge process. The bias circuit can be programmed to control the micro-bridge temperature. The analog output voltage of the bias circuit is connected to the 8b A/D which digitizes the analog output voltage in the range defined by the externally-applied voltages VH and VL. The digital output channel consists of three lines: an input clock, a serial data output, and an output sync signal. The chip requires ±5V supplies and provides TTL-compatible signal levels. Figure 4 shows a micrograph of the 4.0x4.5mm chip. A sketch of the bias circuit is shown in Figure 3b. In it a differential amplifier with gain G and two MOS source followers in a feedback loop. The non-linear microbridge resistor Rref(V1) is connected to the source of M1, and a reference resistor Rref is connected to the source of M2. M1 and M2 are ratioed so that the ratio of gains of M2 to M1 is K.

The operation of the circuit relies on the nonlinear IV curve of the microbridge. In the idealized condition when $V_{in} = 0$, the voltages V1 and V2 are identical; hence the currents through M1 and M2 are ratioed by the factor K. This causes the output of the chip to adjust V1 such that the condition $R_{bias}(V1) = KR_{ref}$ is satisfied. The resistance of the microbridge (and thus its average temperature) is held constant. Hence this circuit is referred to as a constant-resistance (or constant-temperature) circuit. An advantage of this circuit is that its output voltage V1(P) is independent of the supplies.

In the programmable version of the circuit, the MOSFET ratio K is controlled by the bias bits B0 through B2 which connect (or disconnect) a set of binary-ratioed devices in parallel with M2.

The external capacitor C in Figure 3b limits the overshoot on the microbridge temperature when V1(P) is modified as a result of a change in the absolute gas pressure. The circuit has two equilibrium points: either a stable focus (damped oscillatory behavior) or a stable node (non-oscillating transient), depending on the size of $C_{on}$ at the desired bias condition. In addition, there is an unstable node at the origin which is removed by assuring that both V1 and V2 are greater than zero.

Figure 5 shows the final nMOS configuration of the constant-resistance bias circuit. The current $I_{bias}$ of the differential pair is adjusted by the bias network so that the common-mode output voltage of the differential stage $V_{cm}$ is nearly equal to $V_{ref}$. This type of circuit has been shown to be very sensitive to process variations, a desirable condition for circuits fabricated in experimental processes. The loop $L_{bias}$ removes the undesired unstable saddle point at the origin.

Figure 6a shows the measured curve of analog output voltage with a microbridge temperature of roughly 100°C above the substrate. The output voltage experiences a 2V swing for a change in absolute pressure of ambient nitrogen between 10 and 10^14 Pa. The signal flattens out at low pressures because the pressure-independent heat conducted through the beam cross section eventually dominates over the transmission through the gap. Figure 6b shows the digital signals at the chip output for a sampling rate of 1kHz.

Acknowledgments:
This work was partially supported by SRC under contract 90-DC-008. C. H. Mastrangelo was supported by an AT&T Fellowship during the course of this research.

References
Figure 1: Pressure transducer cross-section

Figure 2: SEM micrograph of a microbridge

Figure 3: (a) Chip architecture (b) Constant-resistance bias circuit

Figure 4 — See page 315

Figure 5: nMOS implementation of bias circuit

Figure 6: (a) Output voltage vs absolute pressure (b) Digital signals on the chip operating at 1k samples/s.