ABSTRACT

A thermal absolute pressure sensor of the heated microbridge type has been integrated with an active bias circuit and an 8-bit successive-approximation register (SAR) analog-to-digital (A/D) converter. The chip, which contains about 1000 MOSFETs, measures absolute gas pressure between $10^3$ to $10^4$ Pa, and it is implemented in a 14-mask, 4-μm NMOS technology merged with the microsensor process. Details of the circuit design and layout for this chip have been presented at the 1991 IEEE Int. Solid-State Circuit Conference [1]. This paper describes the fabrication process and sensing performance of the μ-pirani gauge.

MICROBRIDGE AS A PRESSURE SENSOR

Thermal conductivity absolute-pressure sensors are widely used in vacuum systems. Their operation is based on the pressure dependence of the heat transfer from a suspended hot filament through a gas. The filament temperature and IV curve are dependent on the heat transfer and hence on the gas pressure [2]. Recently, microbridge resistor structures consisting of a resistive doubly supported beam suspended above the substrate have been used to detect absolute gas pressure [3]. The pressure-dependent heat transfer in these structures occurs across the gap between the beam and the substrate as shown in the cross section of Figure 1. Figure 2 shows representative IV curves of a polycrystalline silicon microbridge immersed in air at various absolute pressures. At very high pressures, the heat loss through the gas is large; hence there is little heating of the microbridge which results in a nearly linear IV characteristic. At very low pressures, the microbridge temperature is considerably higher than the substrate temperature yielding a nonlinear IV characteristic due to the temperature coefficient of its resistivity (TCR). The change in the IV curves with pressure can be interpreted as a measure of the absolute gas pressure.

CHIP ARCHITECTURE

Figure 3 shows the organization on-chip of the microbridge sensor, constant-resistance bias circuit, and folded-resistor string [4] 8-bit A/D converter. The output of the chip is a robust digital signal representative of absolute pressure that can be transmitted through a noisy channel without any loss in resolution. The circuits are implemented in a robust 4-μm NMOS technology merged with the microbridge fabrication sequence. A robust circuit technology is an essential requirement for an experimental process chip.

The bias circuit can be programmed to control the microbridge temperature. The analog output voltage of the bias circuit is connected to the 8-bit A/D which digitizes the analog output voltage in the range defined by the externally applied voltages VH and VL. The digital output channel consists of three lines: an input clock, a serial data output, and an output sync signal. The chip requires ±5V supplies and provides TTL-compatible signal levels. Figure 4 shows a photograph of the 4.0 × 4.5 mm$^2$ chip.

![Figure 1. Cross section of a microbridge.](image)

![Figure 3. Chip architecture.](image)
Figure 4. Chip photo

Figure 5 shows a simplified non-programmable NMOS configuration of the constant-resistance bias circuit. The circuit adjusts the microbridge voltage such that its resistance is equal to that of the reference resistor [1]. An advantage of this circuit is that its output voltage is independent of the supply [1]. The circuit bias network maintains a constant common-mode output voltage $V_{cm}$ of the differential stage. This type of circuit biasing has been shown to be very insensitive [5] to process variations, a desirable condition for circuits fabricated in experimental processes [6].

The A/D converter consists of a folded 256-tap diffused resistor string, a comparator, and an 8-bit static-logic SAR. This design was chosen for its simplicity, small area requirement, and inherently monotonic conversion [4].

**Figure 5.** NMOS constant-resistance microbridge bias circuit.

**Fabrication**

Figure 6(a) shows a top view of a microbridge, bonding pad and MOS device at the end of the fabrication process. Figures 6(b)-6(f) show longitudinal (L-L) and transversal (T-T) cross sections of Figure 6(a) after the main steps of the 14-mask process.

The process begins with <100> p-type wafers. Next, a conventional LOCOS NMOS process with 0.6 μm of phosphosilicate glass (PSG) isolation is performed on the samples up to the stage where the source/drain contact holes are ready to be opened. A 100 nm film of slightly tensile low residual-stress LPCVD silicon nitride [7,8] is then deposited, and both nitrile and PSG films are plasma etched down to the Si substrate on the areas where the microbridge is fabricated. The thin nitride film protects the MOSFETs from subsequent etching steps [9]. The resulting structure is shown in Figure 6(b). A 0.5 μm spacer layer of a+ polysilicon is then deposited and wet etched as shown in Figure 6(c).

A 0.3 μm layer of low-stress silicon nitride is then deposited which will form the base of the filament. After the deposition, 1 μm of a+ polysilicon is grown. The polysilicon filament is then patterned with plasma etch, stopping at the nitride layer. The resistivity of the polysilicon film was $10^{-5} \, \text{ohm} \cdot \text{cm}$ with a TCR of $9 \times 10^{-4} \, \text{C}^{-1}$. A 0.3 μm layer of low-stress silicon nitride is deposited to form the upper part of the filament seal. Both nitrile layers are then plasma etched down to the first polysilicon spacer as shown in Figure 6(d). Also at this stage the contact holes of the microbridge are opened by the same nitride etch.

The MOSFET contact holes are next patterned. The top layer of silicon nitride on the hole areas is removed with plasma etch, and the PSG under them is etched with 5:1 buffered HF (BHF). The wet etch creates an undercut of the PSG under the nitrile (Figure 6(e)) on the MOS contact holes which requires a conformal metatization such as a contact poly [10] process.

A 0.6 μm spacer layer of a+ polysilicon is then grown on the wafers and wet etched as shown in Figure 6(f). The polysilicon remains on the microbridge as well as on MOSFET areas where it fills the contact-hole undercut. A thin layer (50 nm) of undoped low-temperature oxide (LTO) is deposited, patterned and wet etched. This thin oxide layer prevents aluminum spiking of the following metatization on the poly spacer that covers the microbridge areas. In addition, the thin LTO is left on the bonding-pad areas since it enhances the adhesion of the aluminum metal to the substrate.

A 1.2 μm layer of AlSi alloy is sputtered on the samples and the metal is patterned. The contact polysilicon of the samples is then plasma-etched in SF$_6$ using the AlSi metallization as a mask. The resulting self-aligned contact poly metatization is shown in Figure 6(g).
that the contact poly follows the AISi conformally, and that there is no contact poly under the bonding-pad areas.

A three-layer [10] oxide-passivation layer is then applied to the wafer to protect the metallization. The passivation consists of 0.1 μm of PECVD silicon dioxide, two 0.3 μm layers of high crack-resistance Allied Chemical 3100 siloxane-type spin-on-glass, and 0.5 μm of PECVD oxide on top. The passivation is then patterned and plasma-etched with two lithographies on both the wire bonding areas and the microbridge areas. In the first, the etch stops at the AISi layer while in the second the etch stops at the second polysilicon spacer as shown in Figures 6(h)-(l). After wafer scribing, the samples are immersed in Ethylenediamine-pyrocatechol-water (EPW) anisotropic silicon etch which removes the polysilicon spacers and etches the silicon substrate releasing the microbridge.

Because the AISi of the bonding pad rests on LTO, it does not peel off [11] from the substrate; however it is partially attacked by the silicon etch with only 0.5 μm of AISi remaining on the pad after the etch is completed. The resulting final structure is shown in Figure 6(j). Figures 7(a) and (b) show SEM photographs of typical microbridges, fabricated using this process. Note the sharp plasma-etched edge of the oxide passivation. The microbridges are pulled flat by the slight tensile stress of the low-residual-stress nitride coating [8]. Figure 8 shows an SEM of a 400×3×1 μm³ microbridge suspended over a 25 μm-deep V-groove etched into the substrate and the associated bias circuits.

**MEASUREMENTS**

Several chip samples were placed in a vacuum system with feedthroughs. The vacuum chamber was then pumped down and the output voltage of the chips were recorded. Figure 9 shows the measured curve of the analog output voltage of the circuit with a microbridge temperature roughly 100 °C above that of the substrate. The output voltage experiences a 2 V swing for a change in absolute pressure between 10 and 10³ Pa in a nitrogen atmosphere with a maximum sensitivity of 2 V/decade. The signal flattens out at low pressures because the pressure-independent heat conducted through the beam cross section eventually dominates over the transmission through the gap [12].

A sample chip was placed inside an oven to record the fluctuations of its analog output voltage as a function of ambient (and substrate) temperature. The observed voltage-temperature dependence was less than 2 mV°C⁻¹.

The long-term stability of the circuit was also tested. The analog output voltage of a chip operated at room conditions was recorded for several weeks. The observed signal drift was about 50 μV/day.

Figure 10 shows the digital signals at the chip output for a sampling rate of 1 kilosample per second. The chip power dissipation was 20 mW at this sampling frequency.
Figure 11 shows the linearity error of the A/D converter. Note that there are no missing codes in the conversion.

CONCLUSIONS

We have designed a fully integrated absolute gas-pressure meter with a microbridge, a constant-resistance bias circuit, and an 8-bit A/D converter, all on the same substrate. The chip is fabricated entirely using IC process technology without any hybrid steps. The chip provides a robust digital signal that is representative of the absolute pressure. The sensitivity range of the device presented here is between 10 and 10^6 Pa. The level of integration of this chip corresponds to a MSI sensor chip, thus demonstrating the compatibility of microbridge technology with medium-scale microelectronic circuits.

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