SURFACE MICROMACHINED CAPACITIVE DIFFERENTIAL PRESSURE SENSOR WITH LITHOGRAPHICALLY-DEFINED SILICON DIAPHRAGM

C. H. Mastrangelo\textsuperscript{1}, X. Zhang\textsuperscript{2}, and W. C. Tang\textsuperscript{2}

\textsuperscript{1}Center for Integrated Sensors and Circuits, Department of Electrical Engineering and Computer Science
University of Michigan, Ann Arbor, MI 48109-2122, USA
\textsuperscript{2}Ford Microelectronics, Inc., 9965 Federal Drive, Colorado Springs, CO 80921-3698, USA

SUMMARY

A capacitive surface micromachined sensor suitable for the measurement of liquid and gas pressures was fabricated. The structure consists of a polysilicon stationary electrode suspended 0.7 \( \mu \)m above a 20 \( \mu \)m-thick lightly-doped silicon diaphragm formed by a patterned etch stop. The a-priori patterning of the buried etch stop yields diaphragm widths independent of wafer thickness variations with excellent alignment. The design described here has a pressure range of 100 PSI, a nominal capacitance of 3.5 pF with a full scale span of 0.8 pF and a temperature coefficient of 100 ppm/\( ^\circ \)C. Each device, including a matched reference capacitor, occupies 2.9 mm\(^2\) yielding approximately 2000 devices per 100 mm wafer.

INTRODUCTION

Most low-cost pressure sensors are implemented with piezoresistors. These devices work well but they require extensive calibration and compensation procedures due to their small output signal swing (few mV) and large thermal drifts. Capacitive devices have more controllable characteristics and larger output swings. In this paper a low-cost surface micromachined capacitative sensor for the measurement of differential pressure is presented. Figure 1 shows the cross-section of the device. This design exploits the properties of single crystal silicon for the transducer diaphragm and the versatility of polysilicon micromachining [1] for the fabrication of suspended parts. The sensor consists of a 500 \( \mu \)m-wide, 20 \( \mu \)m-thick epitaxially grown silicon diaphragm, a 3 \( \mu \)m silicon dioxide/nitride passivation layer, 0.7 \( \mu \)m PSG sacrificial layer, and a 3 \( \mu \)m-thick surface micromachined polysilicon reference electrode. A particularly innovative aspect in the construction of the device is the use of a patterned etch-stop layer and subsequent etch-stop removal for precise diaphragm width control and elimination of dopant-induced stress warpage [2]. This step allows us to precisely define the width of the diaphragm with 2 \( \mu \)m accuracy and independently of wafer thickness variations. An identical reference device with no diaphragm is constructed next to the sensing capacitor for a parasitic insensitive capacitance measurement scheme [3]. The dual sensor and reference device occupy an area of 1.5x1.9 mm\(^2\). The sensor has a 3.5 pF default capacitance, a maximum capacitance change of 0.8 pF over a 100 PSI range, and a low temperature coefficient of 100 ppm/\( ^\circ \)C\(^{-1}\). These devices can be manufactured to meet a \( \pm 5\% \) error spec in their \( C-P \) characteristic without any calibration.

PRESSURE SENSOR DESIGN

The device is designed to have a maximum tolerance to process variations and a minimum cost. Ignoring the residual stress, the center load deflection \( z_m \) of the diaphragm is

\[
z_m \approx \frac{\alpha w^3 P}{D}, \quad D = \frac{E t^3}{12(1-\nu^2)}
\]

(1)

where \( D \) is the flexural rigidity of the plate, \( w \) its width, and \( t \) its thickness. The total relative error of the maximum deflection is

\[
\varepsilon_{z_m} \approx \left(16 \left(\frac{\Delta w}{w}\right)^2 + 9 \left(\frac{\Delta t}{t}\right)^2 + \left(\frac{\Delta d}{d}\right)^2 + \left(\frac{\Delta E}{E}\right)^2\right)^{1/2}
\]

(2)

Each of the error components is determined by the accuracy of the transducer dimensions and the material property control. Since a crystalline material is used for the diaphragm, the Young's modulus contribution is negligible. The gap \( d \) can be controlled within 2%. The thickness of the diaphragm is determined by the epitaxy growth control (1\%), and the etch stop typically yielding a cumulative error of 1.5%. The largest contribution is made by variations on \( w \), and it is the dominant error source. In conventional micromachining of bulk pressure sensors, the
diaphragm is etched from the backside. Therefore, the plate width is affected by micrometer variations on the wafer thickness and the \(< 100 > / < 111 >\) etch rate ratio.

This error component however can be eliminated using a patterned etch stop prior to the epitaxy growth. During processing, the backside opening is patterned such that the anisotropic etch yields a 20-40 \(\mu\text{m}\) smaller \(w\). The etch stop is next removed by a p+ etchant resulting in a lateral undercut and a precise diaphragm width as shown in Figure 1. This technique keeps errors in \(w\) under 2 \(\mu\text{m}\) on regular front-side polished wafers.

The selection of \(w, t,\) and \(d\) is an optimization problem with equality and nonequality constraints. Burns [1] described a similar optimization procedure for the design of absolute pressure sensors. We choose the air gap \(d\) such that at the full pressure range, the diaphragm just touches the electrode. Thus we let \(d = z_m(P_r)\) or

\[
d = \frac{\alpha w^4 \rho_r}{D} \tag{3}
\]

The maximum stress in the diaphragm occurs at four midpoints of its edges. This must be smaller than the fracture stress \(\sigma_f\) at the overpressure \(P_{ov}\) yielding a constraint in the aspect ratio of the diaphragm

\[
\frac{w}{t} \leq \sqrt{\frac{\sigma_f}{\beta P_{ov}}} \tag{4}
\]

where \(\beta \approx 0.31\) [4] and for single-crystal silicon \(\sigma_f \approx 600\) MPa is a safe value. The capacitance of the sensor is

\[
C = \frac{\varepsilon_o w^2}{d} \geq C_{\text{min}} \tag{5}
\]

A parameter that needs to be considered is the pull-in voltage of the capacitor [5]. In this structure, the upper electrode is more compliant than the diaphragm, hence it determines this voltage. It can be shown that the pull-in voltage for a clamped elastic plate of thickness \(s\) is

\[
V_p \approx \frac{64}{7} \sqrt{\frac{E s^3 d^3}{5(1-v^2) w^4 \varepsilon_o}} \geq V_{p,\text{min}} \tag{6}
\]

Equation (3) eliminates one of the design variables leaving only three. Also, Eq. (6) tells that the stationary electrode should be as thick as possible to maximize the pull-in voltage. Thus we are only left with two design variables, the diaphragm width \(w\) and its thickness \(t\). The feasible design space is plotted in the \(w-t\) plane of Figure 2 by drawing the curves corresponding to the various constraints. These curves are boundaries of the feasible design region. Equation (4) limits the feasible region to the points in the quadrant below the straight line \(A\). The capacitance constraint of Eq. (5) combined with Eq. (3) yield curve \(B\). The pull-in voltage of Eq. (6) and Eq. (3) yield curve \(C\). Finally, curve \(D\) is the contour of Eq. (2) with \(\varepsilon_r_m \varepsilon_o\). Additional constraints limiting the minimum allowed gap \(d \geq d_{\text{min}}\) are imposed by curve \(E\) since from Eq. (5) we get

\[
w = \sqrt{\frac{C_{\text{min}} d_{\text{min}}}{\varepsilon_o}} \tag{7}
\]

The shadowed area is the feasible design region, and the point \(P\) minimizes the total area yet meeting all the constraints. For this device, the optimum diaphragm is 530 \(\mu\text{m}\) wide, 19 \(\mu\text{m}\) thick with a gap of 0.7 \(\mu\text{m}\). The resulting capacitance is about 3.5 pF per device with a 0.8 pF full scale span.

**FABRICATION PROCESS**

Figure 3 shows the simplified 14 mask fabrication sequence. The process starts with a (100) p-type silicon wafer with a boron concentration of \(10^{15}\) cm\(^{-3}\). An alignment key is first patterned in the front, and the silicon is etched about 1 \(\mu\text{m}\) deep using an SF\(_6\) plasma. The etch-stop areas are lithographically de-
fined and a $2 \times 10^{16} \text{cm}^{-2}$ dose of boron at 100 keV is implanted to form the diaphragm etch-stop. The samples are next annealed at 900 °C for 30 min, in dry O$_2$ to remove implant damage. After removal of the surface oxide, a 20 µm layer of 10$^{15}$ cm$^{-2}$ p-type silicon is grown in a SiH$_4$ atmosphere at 1150 °C. The silane atmosphere minimizes epitaxial pattern shifts [6]. The samples are then ion-implanted with a boron channel-stop implant. Next, a 3 µm layer of LTO is grown as passivation. The LTO is next patterned and etched away in the diaphragm areas with 5:1 BHF. The bottom electrode for the diaphragm is formed by a shallow 10$^{15}$ cm$^{-2}$ arsenic implant. A thin 0.15 µm layer of low-stress silicon nitride [7] is deposited. The nitride layer is next patterned on the diaphragm and contact hole areas and etched in hot H$_3$PO$_4$ using a 0.3 µm-thick LTO mask. After stripping of the mask, a 0.7 µm-thick sacrificial layer of LTO is grown and patterned to define the capacitor gap. A 0.1 µm-thick layer of low-stress nitride was deposited on some of the samples as a dielectric. A 1.5 µm-thick layer of undoped low-stress polysilicon is grown at 600 °C [8]. The poly layer is next implanted with 10$^{16}$ cm$^{-2}$ of phosphorus. A second polysilicon layer 1.5 µm-thick is grown next. The poly samples are next annealed at 900 °C for 30 min to distribute the dopants and patterned using 64:33:3 HNO$_3$ : H$_2$O : NH$_4$F wet etch. A second 0.1 µm layer of nitride is grown on some samples to balance bimetallic stresses. A protective 1 µm layer of LTO is next deposited and stripped on the backside followed by a 0.1 µm layer of low-stress nitride. The backside of the samples is next patterned in a double sided aligner and the opening for the diaphragm etch is formed with SF$_6$. The opening is made slightly smaller than that required for the diaphragm such that the etch stops within the implanted buried layer. Samples are next anisotropically etched in a mixture of KOH-isopropyl alcohol at 80 °C until the etch-stop is reached. Next, the etch-stop is removed by a mixture of 1:3:8 HNO$_3$ : HF : CH$_3$COOH etch for 5-10 min. with a selectivity of about 100:1 respect to lightly-doped material [9]. A feedback system which pours H$_2$O$_2$ periodically into the etch is used to keep the pH and selectivity constant. The resulting diaphragm has been undercut laterally to precise dimensions and alignment to the top structure. The nitride and LTO protective layers are next removed by H$_3$PO$_4$ and 5:1 BHF wet etching followed by a 1000 °C anneal for 30 min. A series of holes is next patterned on the poly reference electrode using SF$_6$ : C$_2$Cl$_2$F$_5$. A few of the holes are next etched to form a 15 µm undercut. The Aluminum metallization is next deposited and patterned. A 5 µm layer of paraxylene [10] is next deposited onto the sample to form “supporting feet.” The paraxylene is patterned with an aluminum mask and O$_2$ plasma as in [10]. Finally, the remaining sacrificial oxide is removed in BHF, leaving the top electrode supported by the paraxylene feet as described in [10]. The samples are then covered with a thick layer of photoresist and are scribed 13 mils deep in the dicing machine. The thick resist is then removed in acetone and the samples are rinsed in DI water to remove the silicon dust from the dicing. Next, the samples are cleaved and the chips diced. The devices are ready for mounting in a package. After mounting, the packaged devices are placed in an oxygen plasma reactor for 1-2 hours at 450W to etch the parylene feet hence releasing the top electrode.

Figure 4 shows a top view of the 500×500 µm$^2$ sense and reference capacitors. The chessboard pattern indicates where the parylene feet were on the top electrode. Figure 5 shows an SEM of the gap between the polysilicon electrode and the epitaxial diaphragm. Figure 6 shows a cross section of a diaphragm near one of the corners showing the undercut of the etch stop. The resulting polysilicon plate to diaphragm registration error is approximately 1.5 µm.

**EXPERIMENTS**

The device capacitance was first measured. The devices show nominal 3.5 pF with values varying from 3.35 to 3.65 pF across the wafer. The matching between adjacent reference and sensing capacitors is better than 1%. Samples with the nitride dielectric showed a polysilicon plate warpage of approximately 0.3 µm at their center while samples without the dielectric showed no warpage. The capacitance-pressure measurement was carried out as follows. The
The device is first bonded to a small 3 × 3 × 3 mm³ block of 7740 glass with a feedthrough orifice. The glass block is bonded to a stainless steel jig with pressure ports. The glass block behaves as a stress buffer zone that decouples the large mismatch between the silicon on the sensor and the stainless steel jig. The device is next pressurized on the diaphragm backside using a N₂ tank. Figure 7 shows a typical response of the sensor over 140 PSI of pressure difference. The capacitance experiences a very large change of 25% of its value over the pressure of interest. The nonlinearity on the curve is the result of the linear dependence of the gap on pressure [5]. The \(\frac{1}{C} \propto P\) characteristic shows a linear dependence on \(P\) on the low pressure regime and a deviation from linearity at high pressures due to the bowed shape of the diaphragm. At even large pressures, the diaphragm contacts the stationary poly electrode which stiffens the diaphragm and producing a decrease in the slope. The temperature dependence of the \(C \propto P\) characteristic was measured. The chip shows an average temperature drift of 100 ppm/°C. This number is well within the expected value for capacitive devices.

CONCLUSIONS

The design, fabrication, and testing of a surface micromachined capacitive pressure sensor is presented. The device consists of a stationary polysilicon electrode suspended 0.7 μm above a lightly-doped epitaxial diaphragm. The diaphragm is patterned using a lithographically-defined implant etch-stop prior to the epitaxial growth. This scheme allows nearly perfect alignment of the epi diaphragm to the poly electrode, and accurate width control independent of wafer thickness. The polysilicon plate flatness was excellent when no dielectrics are used in the capacitor. The devices show a nominal capacitance of 3.5 pF and a 25% change of capacitance over a 100 PSI range.

References