AN ULTRASENSITIVE UNCOOLED HEAT-BALANCING INFRARED DETECTOR

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ABSTRACT

A very sensitive uncooled infrared detector using heat-balancing technique is proposed and tested. The device is fabricated by commercial CMOS foundry plus a post-CMOS releasing step. By employing the heat balancing between the incoming infrared radiation and heater power, the responsivity of this device is controlled by the biasing current. The measured responsivity is about $1.2 \times 10^6$ V/W when the infrared source is chopped at 20 Hz which is two order higher than any other bolometer detector. Since the fabrication is totally CMOS process compatible, low cost and highly sensitive infrared detector can be realized using this technology.

INTRODUCTION

Bolometers are thermally isolated detectors that are heated by infrared radiation absorbed on their surface. The temperature raise is converted to an electrical signal by use of a thermistor element. Infrared bolometer detectors are widely used for night vision systems, thermal targeting, and motion sensing. The most sensitive bolometers are superconductive devices since they have high responsivities and low noise at cryogenic temperatures. Often their cooling system is heavy and bulky hence these devices are not adequate for light weight and portable systems. Recent work by Honeywell [2] and Texas Instruments [3] has demonstrated the feasibility of uncooled bolometric devices. Honeywell’s device used a micromachined array of microbridge type bolometric pixels 50 $\times$ 50 $\mu$m$^2$ each. The temperature detector was a vanadium oxide resistor $V$O$_2$ patterned on the microbridge which has a sharp transition in its resistance near room temperature. The Texas Instruments device uses a pyroelectric pixel of barium strontium titanate (BST) that is patterned directly on the substrate. Both devices have a plane of interfacing electronics for multiplexing of the pixel signals. However, these system suffers from the responsivity is highly dependent on the process parameter due to working principle used is open loop structure. The calibration and cost of these detector will take a lot of effort.

In this paper we report the fabrication and testing of an ultrasensitive uncooled silicon infrared detector based on electrothermal feedback principles [1]. The structure is fabricated using simple post-processing micromachining of a conventional MOSIS CMOS wafer; yet it provides a performance comparable to much more complex detectors [2] [3].

DESIGN AND FABRICATION

The closed-loop heat balancing scheme is described in Fig. 1.

![](image)

**Fig.1 Closed-loop bolometer system**

The basic idea is the incorporation of a heat balancing element in each pixel. The thermistor is now connected to a comparator and a gain stage that powers the pixel heater. A closed feedback loop is established through the thermal coupling between the heater and the thermistor element that keeps the pixel temperature constant. Since the pixel temperature is kept constant, so is the total power heating the pixel. Thus, any increase in the incident power of incoming infrared radiation must be exactly balanced with a decrease in the electrical power dissipated by the pixel heater. In particular, if the heater is implemented as a current source then there exist a linear relationship between the voltage of the heater and the incident radiation power. Furthermore this relationship is set by the heater current. The sum of the incident and generated power is constant

$$Q_{\text{heater}} + Q_{\text{rad}} = \text{constant} \quad (1)$$
Differentiating Eq. (1) and using $Q_{\text{heater}} = I_0 V_0$ where $I_0$ is constant, we obtain

$$dQ_{\text{heater}} + dQ_{\text{rad}} = I_0 dV_0 + dQ_{\text{rad}} = 0$$

hence the responsivity $R$ of the pixel is

$$R = \frac{dV_0}{dQ_{\text{rad}}} = -\frac{1}{I_0}$$

This relationship is exact and independent of any device parameters. For example, Eq. (3) yields a high responsivity of $10^6$ V/W with a 1 $\mu$A heater current.

A schematic of the detector structure and circuit is shown in Fig. 1. The PMOS devices M4 and M5 are placed under a common suspended well thermally isolated from the substrate hence their characteristics are susceptible to heating caused by absorbed incoming radiation. The electrothermal detector operates as follows. MOSFETs M2 and M3 essentially form a high impedance current source referenced to $I_b$. Since the PMOS devices are thermally isolated, this bias current raises the suspended well temperature 1-5 $^\circ$C above the substrate. MOSFET's M6-M9 form a low-frequency bias feedback loop that stabilizes the voltage at node (1) at 1/2 of the supply voltage hence maintaining all devices at saturation at the quiescent point.

![Fig. 1: Schematic of the IR detector](image)

When heat radiation is suddenly absorbed by the suspended well, due to its high thermal isolation, the well temperature increases. If $I_b$ is sufficiently low, this temperature increase induces a reduction of the threshold voltage $V_T$ in M4 and M5 provided $I_b$ does not exceed few $\mu$A's $[4, 5]$. Since the gate voltage of M1 is essentially fixed due to the low frequency pole of the biasing circuit, the transient $V_T$ reduction tends to increase M5's current. This positive temperature coefficient of the drain current (TCI) is experimentally shown in the $V_C$ vs $\sqrt{I_d}$ curve of Fig. 2. Since the current in this branch is limited by $I_b$, the circuit responds instead by decreasing the voltage drop across well devices M4 and M5 yielding a net reduction on the well power dissipation hence a drop in the well temperature. This phenomena in fact constitutes an electrothermal feedback loop that tends to maintain the temperature of the well constant.

![Fig. 2: MOS current dependence vs. temperature](image)

The electrothermal behavior of the detector is essentially modeled by the equivalent electrothermal circuit of Fig. 3 consisting of coupled electrical and thermal branches. Source $v_T$ represents the change in $V_T$ with well temperature, $g_{m5}$ and $r_n$ are the transconductance of M5 and the output impedance at node (1). Source $I_{th} = I_b v_1$ represents changes in well power dissipation and, $R_{th}$ and $C_{th}$ are the thermal resistance and capacity of the well. Provided the loop gain is high enough, the electrothermal transfer function of this detector, or responsivity is exactly $R = 1/I_b$. Thus for a bias current of 1 $\mu$A, this device should yields a responsivity of $10^6$ V/W.

The absorber layer was realized using the second metal layer in conventional CMOS process. This metal is encapsulated by the passivation silicon nitride and oxynitride layer. This kind of absorber can not achieve the high absorptance as some metal black usually used in other infrared detector technology $[7]$. However, it can still achieve around 20% ~ 30% absorptivity $[8]$. It can also be a blocking layer preventing the photo effect induced by any other light sources.
The infrared detector was constructed by releasing the n-well of a 1.2 μm CMOS wafer as shown in Fig. 1(a) using an electrochemical etch stop technique described by Reay [6]. Fig. 4 shows an SEM of the 22×35 μm² detector well suspended by four 50×5 μm² oxide passivated polysilicon beams which serve as interconnect lines from the well to the substrate. A metal plate covers the suspended well PMOS devices to suppress any photoresponse. The 6-transistor, 109 × 109 μm² pixel was released in a TMAH mixture of 10 wt. % heated at 80 °C for 1-1.5 hrs.

Fig. 4: SEM of detector showing suspended well

**TESTING SETUP AND RESULTS**

The devices were tested in the setup shown in Fig. 5 consisting of a light source, a light chopper and a SR830 lock-in amplifier (Stanford Research Instruments). The light source was an incandescent bulb enclosed inside a metal case with a silicon window. The radianc of the light source was measured using a Molecron P-42 pyroelectric detector calibrated using an 835 nm SpectraDiode labs laser diode and a Newport 1815-C power meter.

Initial measurements show a responsivity of \( R \approx 1.1 \times 10^6 \text{ V/W} \) at atmospheric pressure with a noise equivalent power \( \text{NEP} < 3 \times 10^{-10} \text{ W/√Hz} \). The normalized detectivity is

\[
D^* = \frac{(4\pi f \Delta f)^{1/2}}{\text{NEP}}
\]

The measured detectivity \( D^* = 10^6 \text{ cm} \sqrt{\text{Hz W}^{-1}} \) at the 30 Hz. Which is comparable to the commercial infrared detector. Fig. 6 shows the responsivity as a function of frequency at a bias current of 800 nA. The responsivity is decreased inversely proportional to the frequency. It is due to the thermal pole of the this electrothermal feedback loop.

Fig. 5: Experimental apparatus used for the responsivity measurements

Fig. 6: Responsivity vs. chopper frequency

Fig. 7 shows the responsivity as a function of the bias current. The responsivity is not inversely proportional to the operating current as we expected. The main reasons for this curve. First, the overall power gain after
passing through the electrical thermal feedback is not higher than 1 thus the detector does not behave like what was derived in Eq. (3). In vacuum testing (650 mTorr), the responsivity is about 2 ~ 3 times higher than what we measured in atmospheric condition. It is due to the less thermal loss in vacuum. The power gain is expected to be higher. It is still not high enough to realize the inversely proportional to current relationship. It is also anticipated that if the zero temperature coefficient point of the transistor can be increased by changing the design parameter. By this change, the power gain of the electrical thermal loop can be much higher than 1 and the expected $R = 1/I_b$ can be performed. Fig. 8 shows a scope trace of the output signal at 40 Hz.

An untrasensitive thermal infrared detector based on heat-balancing technique is presented. It has the very high responsivity which is 2 order better than other commercial detector. It is also CMOS process compatible which can reduce the production cost of this type of detector. It also allow on chip signal processing and occupied less area than thermopile based detector which can result in higher resolution in the infrared imaging array. The development of imaging array is undergoing using this technology and design described in this paper.

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References


