CMOS Uncooled Heat-Balancing Infrared Imager

C. C. Liu and C. H. Mastrangelo

Abstract—In this paper we report the fabrication, design and testing of an uncooled 8 × 8 infrared imager based on an active pixel heat balancing technique. The imager is fabricated using a commercial CMOS process plus a simple electrochemical etch stop releasing step. The basic active pixel detector structure consists of a simple cascode CMOS amplifier in which the PMOS devices are built inside a thermally-isolated floating n-well. The intrinsic coupling of the cascode currents with the self heating of the well forms an electrothermal feedback loop that tends to maintain the well temperature constant. By employing the heat balance between incoming infrared radiation and the PMOS device power dissipation, the responsivity of the detector is controlled by the cascode biasing current. Measurements show responsivities between 0.3-1.2 × 10^6 V/W when the infrared source is chopped at 20 Hz and a detectivity D* = 3 × 10^7 cm^1/2 Hz W^−1 at 30 Hz. Noise measurements suggest that a D* of 10^8 cm^1/2 Hz W^−1 is achievable in this design.

I. INTRODUCTION

Bolometers are thermally isolated detectors that are heated by infrared radiation absorbed on their surface [1]. The temperature raise is converted to an electrical signal using of a thermistor element. Infrared bolometer detectors are widely used for thermal targeting, night vision systems, and motion sensing. The most sensitive bolometers available are cryogenically cooled superconductive devices. Often their cooling system is heavy and bulky; hence these devices are not adequate for light weight and portable systems. In addition, the cryogenic cooler is the most expensive component in the photon detector IR camera, and has finite lifetime only around 2,000 hours.

Recent work by Honeywell [2] and Texas Instruments [3, 4] has demonstrated the feasibility of uncooled bolometric devices. Honeywell’s device used a micromachined array of microbridge type bolometric pixels 50 × 50 μm^2 each. The temperature detector was a VO_2 resistor patterned on the microbridge which has a sharp transition in its resistance near room temperature. Similar technology has been applied into different developed commercial available infrared imagers [5, 6]. The Texas Instruments device uses a pyroelectric pixel of barium strontium titanate (BST) that is patterned directly on the substrate. Both devices have a backplane of interfacing electronics for multiplexing of the pixel signals. Recently, the research work has been concentrating on the monolithic fabrication of infrared detector using micromachining techniques [7] which trade the fill factor with potential high yield and lower production cost. In all of these technologies [8–10], the infrared detectors have highly process dependent responsivities and offsets requiring elaborate calibration procedures and the extensive use of corrective electronics.

Many of these problems can be potentially avoided if the detector balances the incoming heat actively thus establishing a direct correspondence between the incoming heat and its electrical output. In this paper, we report the design, fabrication and testing of an active uncooled infrared detector based on electrothermal feedback principles [11]. The detector operates by approximately balancing the incoming heat with a reduction in its internal power generation. The latter can be directly measured thus providing a relatively well-controlled output response. The heat balancing detector is implemented with an MOS amplification stage built on a suspended n-well of a conventional CMOS process.

The chief trade off of this technique, namely a higher noise floor that is a consequence of the necessary amplification electronics, is also discussed below. The paper begins with a comparison of open and closed loop detector configurations followed by a description of the heat balancing pixel detector, its fabrication, test and the implementation of a simple prototype 8 × 8 imager.

II. OPEN LOOP DETECTION

Most conventional bolometers operate in the open loop scheme shown in Fig.1. Upon the absorption of incident radiation, the thermally isolated plate temperature increases changing the electrical characteristic of the thermistor. The electrical signal of the thermistor is typically amplified yielding voltage V_o representing the power of the incoming radiation. One of the major problems with this mode of operation is that the measured signal is influenced by many material properties, offsets and drifts which make the response difficult to predict.

For example in the simple open loop detector circuit shown in Fig.2, the bolometer R_d with temperature coefficient of resistance α is connected through biasing resistor R_1 to the voltage
source V. For incident power $\Delta \Phi$ the bolometer temperature increase $\Delta T_d$ obeys

$$C \frac{d \Delta T_d}{dt} + G_0 \Delta T_d = W_h + \Delta \Phi$$  \hspace{1cm} (1)$$

where

$C$ = the heat capacitance of the bolometer element
$G_0 \Delta T_d$ = the conductive and radiative heat flow for the element
$W_h$ = the self generated thermal power in the bolometer

The responsivity of this detector circuit [12] is

$$R = \frac{\Delta V_o}{\Delta P_s} = \frac{I \xi_R \alpha}{G_0 (\infty + \omega \tau \xi) \alpha}$$  \hspace{1cm} (2)$$

where

$$G_e = G - \alpha G_0 (\Delta T_d) \left( \frac{R_1 - R_d}{R_1 + R_d} \right), \quad \tau = C/G_e$$  \hspace{1cm} (3)$$

and

$G_e$ : effective thermal conductance
$G$ : thermal conductance for a small temperature change
$\xi$ : the emissivity of the bolometer
$\omega$ : sinusoidal radiation input frequency

The responsivity thus depends on the material properties like $\alpha$, and $R_d$ that vary from run to run hence a calibration procedure is needed. In a focal plane imaging array, this must be done for each pixel in the array.

III. HEAT-BALANCING DETECTOR

A. Closed Loop Infrared Sensing Scheme

The sensing scheme used in our detector is shown in Fig. 3. The basic change consists of the addition of a heat balancing element (a heater) in the thermally isolated area. The amplified thermistor output powers the balancing heater; thus a closed electrothermal feedback loop is established by the thermal coupling of the heater-induced temperature raise and the thermistor response. If the the loop gain is high enough, this configuration keeps the detector temperature and the total power of the plate constant. Thus, any increase in the incident power of incoming infrared radiation must be balanced with a corresponding decrease in the electrical power dissipated by the heater [13].

If the heater is implemented as a current source then there is a linear relationship between the voltage of the heater and the incident radiation power. Furthermore this relationship is set by the heater current. Since the sum of the incident and generated power is constant

$$Q_{heater} + Q_{rad} \approx \text{constant}$$  \hspace{1cm} (4)$$

Differentiating Eq. (4) and using $Q_{heater} = I_o V_o$ where $I_o$ is constant, we obtain

$$dQ_{heater} + dQ_{rad} = I_o dV_o + dQ_{rad} = 0$$  \hspace{1cm} (5)$$

hence the responsivity $R$ of the pixel is

$$R = \frac{dV_o}{dQ_{rad}} \approx -\frac{1}{I_o}$$  \hspace{1cm} (6)$$

This relationship is independent of any device parameters hence the detector response is well defined. For example, Eq. (6) yields a high responsivity of $10^6$ V/W with a 1 $\mu$A heater current. The inverse current relationship can only be obtained if the electrothermal open loop gain is sufficiently high.

The electrothermal loop consist of three different unit conversion stages shown in Fig. 4. Stage $G_{PT}$ converts changes in the detector power $\Delta P_e$ to temperature fluctuations $\Delta T_e$. The thermal loss to the ambient determines the conversion efficiency; hence the higher the thermal isolation the larger $G_{PT}$ is. Stage $G_{TV}$ represents a temperature sensor that converts temperature excursions to a voltage signal $\Delta V$. Stage $G_{VP}$ amplifies $\Delta V$ and converts it to a compensating power $-\Delta P_g$ through using a constant current load.

The overall loop gain $\Gamma$ is

$$\Gamma = G_{PT} \times G_{TV} \times G_{VP} = \frac{\Delta P_g}{\Delta P_e}$$  \hspace{1cm} (7)$$

If $\Gamma \gg 1 \Rightarrow \Delta P_e \approx 0 \Rightarrow \Delta T \approx G_{PT} \Delta P_e \approx 0$$  \hspace{1cm} (8)$$

A high gain product ensures that the error power $\Delta P_e$ and the temperature difference $\Delta T_e$ are small. However not all of these terms are large. $G_{PT}$ can be as large as $10^5$ K W$^{-1}$, but for most thermistors $G_{TV}$ is usually just $\approx 10^{-3}$ V K$^{-1}$, and the last term $G_{TP}$ is

$$G_{VP} = A_v I_o \approx 10^{-6} A_v \ \text{WV}^{-1}$$  \hspace{1cm} (9)$$

where $A_v$ is the voltage amplification of the last stage. In order for the loop gain to be substantial, a large $A_v \approx 10^4$ is necessary within each detector. This can be achieved using a CMOS cascode gain stage as explained below.
B. Thermistor Implementation Using MOSFET

Thermistor elements can be implemented using passive or active devices. Two parameters are important for their use in infrared detectors. First, the temperature coefficient must be as large as possible, and second the element must have a low noise which ultimately determines the minimum detectable signal.

In our detector the choice of thermistor element is constrained to materials and devices that can be built on the n-well of a conventional CMOS process. It can be achieved in a number of ways using resistors or diodes, but eventually the thermistor signal must reach the gate of a fairly high gain MOSFET amplifier. Therefore we are noise limited by the MOS device performance with a substantial amount of 1/f noise.

In our detector we use the same PMOS device for thermistor and amplification purposes since the characteristics are temperature dependent. From the simple model for the MOSFET drain current operated in saturation with strong inversion

$$I_{DS} = \frac{1}{2} \mu C_{OX} (V_{GS} - V_T)^2$$  \hspace{1cm} (10)

two parameters: threshold voltage $V_T$ and surface mobility $\mu$ in Eq. (10) are temperature dependent. The threshold voltage of a PMOS devices can be expressed as following [14]:

$$V_T = V_{FB} + 2 |\phi_p| - \frac{Q_d}{C_{ox}}$$  \hspace{1cm} (11)

where $V_{FB}$ is the flat band voltage, $\phi_p$ is the Fermi potential of the p-substrate, $Q_d$ is the charge per unit area contained within the surface depletion region and $C_{ox}$ is the oxide capacitance per unit area. The temperature sensitivity of the threshold voltage can be determined by exploring the temperature effects for each term in the equation listed above. Empirically, the threshold voltage variation from the ambient temperature fluctuation can be approximated modeled by a simple linear function as:

$$V_T(T) = V_T(T_0) - \alpha (T - T_0)$$  \hspace{1cm} (12)

where $\alpha$ is approximately about $1 \sim 2 \text{mV/°C}$ for regular CMOS process fabricated devices. This expression is valid over the range of 200 to 400 K, where $\alpha$ depends on the substrate doping level and the dosage of implants used during fabrication.

In MOSFET, the channel mobility is a strong function of temperature change. The temperature coefficient of surface mobility is empirically extracted as following [15]:

$$\mu(T) = \mu_0 \left(\frac{T_0}{T}\right)^n$$  \hspace{1cm} (13)

The temperature dependence of surface mobility is proportional to $T^{-n}$ where $n$ ranges from 1 to 2.5, depending on the oxide growth condition and temperature range.

The threshold voltage and mobility coefficients tend to cancel each other. Therefore, the temperature coefficient of drain to source current depends on which temperature effect dominates at a given bias point. Further there is a bias point at which these two effects cancel out resulting in a zero temperature coefficient (ZTC) [16, 17]. The ZTC point depends on the size of transistor, oxide thickness, temperature coefficient of threshold voltage and surface mobility.

Fig. 5 shows the I-V-T characteristics of a PMOS device ($L=4.2 \mu m$, $W=8.4 \mu m$) using a MOSIS 1.2 $\mu m$ N-well HP CMOS process current over the temperature range from 25 °C to 100 °C.

C. Basic detector circuit

Fig. 6 shows the basic implementation of the heat balancing bolometer. M1 is the thermistor element, and the combination of M1 and M2 form a cascade amplification stage and heater. Both devices are placed on a thermally isolated well suspended through oxide-isolated polysilicon beams that also carry electrical leads to the chip substrate.

Fig. 7 shows a schematic of the typical detector structure. PMOS devices M1 and M2 are covered by a layer of second metal used as a light shield for suppressing any photo effect. The detector absorber layer was realized using the second metal layer covering the well region. This metal is covered by silicon nitride and oxynitride passivation layers. This type of absorber can typically achieve a 20% ~ 30% absorptivity [18, 19].

The detector circuit is biased by current $I_b$ in a regime that makes the temperature coefficient of current in M1 positive (ie. $I_b \leq 1 \mu A$). This current also determines the detector responsivity. In order to achieve a high loop gain, gate bias voltages $V_G$ and $V_{ref}$ are adjusted such that both transistors are in saturation.
Note that a small but significant bias power \((V_{dd} - V_1)I_b\) is dissipated on the well; therefore the well temperature normally rests a 1-5°C higher than the substrate. Upon the absorption of radiation, the well temperature increases causing the threshold voltage of M1 to decrease; hence the current of M1 tends to increase. However, the current through M1 and M2 can not exceed \(I_b\). Therefore the circuit responds by pulling up voltage \(V_1\) instead decreasing the power dissipation of M1 and M2 and reducing the temperature of the well close to its original value. If the loop gain large enough the detector noise equivalent voltage \(V_{ref}\) is generated by MOSFETs M6-M9. These transistors monitor \(V_1\) cutting off M1 if \(V_{dd} - V_1 < 2|V_{TP}|\). This maintains M1 and M2 in saturation if \(V_{GS1}\) and \(V_{GS2}\) are small.

The stabilization circuit must track variations on gain, threshold voltage, and substrate temperature, but it should not interfere with the incoming infrared signal. The signal isolation is implemented by the insertion of a low frequency pole which short out the stabilization loop at high signal frequencies. The modulation of the radiation is also beneficial to remove much of the \(1/f\) noise present in the MOSFETs.

The frequency response of the detector circuit is calculated from the equivalent electrothermal network of Fig.9. Source \(v_T = \alpha \Delta T\) represents the change in \(V_{TP}\) with well temperature, \(g_{m1}\) and \(r_o\) are the transconductance of M1 and the output impedance at node (1). Source \(Q_T = I_b v_1\) represents changes in well power dissipation, and \(R_T\) and \(C_T\) are the thermal resistance and capacity of the suspended well. The error voltage \(v_e\) represents small signal changes to \(V_{GS1}\).

\[
\Delta V_T = 4 k_B T_d G_{th} \Delta f
\]

where \(k_B\) is Boltzmann’s constant, and \(\Delta f\) is the measurement bandwidth. In general for the structure of Fig. 6, the NEP is dominated by the \(1/f\) mosfet noise [20]

\[
\overline{v^2}(f) \approx \frac{K_f L W \mu}{2 C_{ox} W L f} \Delta f
\]

where \(\mu\), \(C_{ox}\), \(W\), and \(L\) are the mosfet mobility, gate capacitance per unit area, width and length, respectively. Therefore to minimize the NEP, M1-M5 should be made as large as possible.

\[
NEP^2 \approx \frac{\Delta \Phi^2}{R^2} + \left( \frac{2 \overline{v^2}}{\overline{v^2}} + \frac{\overline{v^2}}{R^2} \right) (14)
\]

where \(\Delta \Phi^2\) is the mean square fluctuation in radiation power, and \(\overline{v^2}\) and \(\overline{v^2}\) are the input referred noise equivalent voltages of the M5-M4 NMOS and M1 PMOS devices.

The mean power fluctuation is just a function of the operating temperature \(T_d\) and thermal conductance \(G_{th}\) of the thermally isolated detector (and plate) [12]

\[
\Delta \Phi^2 = 4 k_B T_d G_{th} \Delta f
\]

\[
\overline{v^2}(f) = \frac{k_B}{2 \mu C_{ox} W L f} \Delta f
\]

E. Biasing

Any practical implementation of the detector of Fig. 6 requires additional bias stabilization circuits for several reasons. First, because of the high cascode gain the gate voltage of M1 should be precisely adjusted to maintain M1 and M2 in saturation. Second, once a proper \(V_{G1}\) is determined, any excursion of the substrate temperature would upset the current balance moving M1 out of saturation.

The stabilization of the bias point is accomplished with the circuit shown in Fig.8. Transistors M3-M5 form the bottom half of the cascode and a current mirror for setting \(I_b\). Bias \(V_{ref}\) is set to about \(V_{dd}/2\), and gate voltage \(V_{GS1}\) is generated by MOSFETs M6-M9. These transistors monitor \(V_1\) cutting off M1 if \(V_{dd} - V_1 < 2|V_{TP}|\). This maintains M1 and M2 in saturation if \(V_{GS1}\) and \(V_{GS2}\) are small.

The stabilization circuit must track variations on gain, threshold voltage, and substrate temperature, but it should not interfere with the incoming infrared signal. The signal isolation is implemented by the insertion of a low frequency pole which short out the stabilization loop at high signal frequencies. The modulation of the radiation is also beneficial to remove much of the \(1/f\) noise present in the MOSFETs.

The frequency response of the detector circuit is calculated from the equivalent electrothermal network of Fig.9. Source \(v_T = \alpha \Delta T\) represents the change in \(V_{TP}\) with well temperature, \(g_{m1}\) and \(r_o\) are the transconductance of M1 and the output impedance at node (1). Source \(Q_T = I_b v_1\) represents changes in well power dissipation, and \(R_T\) and \(C_T\) are the thermal resistance and capacity of the suspended well. The error voltage \(v_e\) represents small signal changes to \(V_{GS1}\).
The circuit has two feedback loops. The electrothermal loop \( L_T \) involves \( \Delta T \) and determines the responsivity. The bias stabilization loop \( L_b \) involves \( gm_0 \) and the shorting pole introduced by \( gm_0 \) and \( C_1 \). The response of the circuit at a particular frequency is dominated by the loop with the largest gain. The ratio of open loop gains is

\[
\frac{\Gamma_T}{\Gamma_b} \approx \frac{\alpha I_{th} R_T g m_0 (1 + s C_1/gm_0)}{2 gm_0 (1 + s R_T C_T)} \quad (17)
\]

\[
\approx 10^{-4} \frac{gm_0 (1 + s C_1/gm_0)}{2 gm_0 (1 + s R_T C_T)} \quad (18)
\]

Therefore in order to short the bias loop, \( gm_0 << gm_0 \), or the frequency separation between pole \( gm_0/C_1 \) and the chopped radiation signal must be high. Achieving the latter is difficult because it is difficult to obtain a pole below about 0.1 Hz with on-chip components. Further the high frequency response is dominated by the loading capacitance at node (1) and the thermal capacitance of the suspended well. This limits the maximum signal frequency to about 100 Hz, and the maximum separation to roughly three orders of magnitude.

Alternatively, the voltage required to stabilize the detector bias can be stored in \( C_1 \) momentarily under open loop conditions. This is the approach used in the actual imager discussed in section IV.

F. Fabrication

The infrared detector was constructed by releasing the n-well as shown in Fig. 7 using an electrochemical etch stop technique described by Reay [21]. First, conventional CMOS chips were fabricated using the HP 1.2 \( \mu \)m CMOS MOSIS process. The etch opening is accomplished by superimposing active, contact, via and pad openings in a conventional CMOS layout. The chips were next diced and wire bonded to DIP ceramic packages. The etch release was done by immersion of the packaged chips into the electrochemical etch bath.

The etching solution is 10 wt % tetramethyl ammonium hydroxide (TMAH) with water solution [22, 23] enriched with dissolved silicon. The silicon rich TMAH solution is an anisotropic etchant that penetrates the substrate through the openings undercutting the well. After releasing the well, the etch stops at the <111> silicon crystal planes without attacking the exposed aluminum metal lines.

A four terminal electrochemical etch stop method is used to prevent the n-well being attacked by the etching solution. The N-well is biased at -0.8 V versus etching solution and the p-type substrate is biased at -1.5 V with a potentiostat (EG&G 362). A solid Ag/AgCl reference electrode (In Vivo Metric E271S) is used as the reference electrode and the platinum foil is the counter electrode in conducting the needed current to maintain the potential difference. After the etch, the packaged samples are thoroughly rinsed in DI water and tested.

Fig. 10 shows a photograph of a 28x42 \( \mu \)m\(^2\) detector well suspended by four 56x5 \( \mu \)m\(^2\) oxide passivated polysilicon beams which serve as interconnect lines from the well to the substrate. A metal plate covers the suspended well PMOS devices to suppress any photoresponse. The 8-transistor, 109 x 109 \( \mu \)m\(^2\) pixel was released in a TMAH mixture of 10 wt % heated at 80 °C for 1-1.5 hrs.

G. Characterization

The devices were tested in the setup shown in Fig.11 consisting of a light source, a light chopper and a SR830 lock-in amplifier (Stanford Research Instruments). The light source was an incandescent bulb enclosed inside a metal case with a silicon window. The radiance of the light source was measured using a Moletron P-42 pyroelectric detector calibrated using an 835 nm SpectraDiode labs laser diode and a Newport 1815-C power meter. Initial measurements show responsivities of

\[
R \approx 0.3 - 1.1 \times 10^6 \text{ V/W at atmospheric pressure with a noise equivalent power } NEP/\sqrt{\Delta f} < 3 \times 10^{-10} \text{ W}/\sqrt{\text{Hz}}. \]

For these measurements the bias stabilization circuit was implemented using an external op-amp and filter. The normalized detectivity is

\[
D^* = \frac{(A_d \Delta f)^{1/2}}{NEP} \quad (19)
\]

where \( A_d \) is the detector area. The measured detectivity of \( D^* = 3 \times 10^7 \text{ cm} \sqrt{\text{Hz W}^{-1}} \) at 30 Hz is comparable to that of commercial pyroelectric detectors but smaller than that observed with passive thermistors due to the 1/f noise in active PMOS thermistor and heat balancing heater.

Fig. 12 shows the responsivity as a function of frequency at a bias current of 800 nA. The responsivity decreased roughly inversely proportional to the frequency due to the thermal pole as well as capacitive loading at the detector output.

The detector response was next measured in a vacuum environment at 650 mT. An increased responsivity 2-3 times higher...
than that observed at atmospheric conditions is observed. This behavior is consistent with a reduction on the heat loss and a corresponding increase in the loop gain. The spectral response of the detector to different wavelengths was next measured by placing an IR monochromator (Scientific Measurement Systems MonoSpec 18) between the light source and the detector. The detector response was next normalized to that of the calibration detector. The responsivity shows absorption peaks near 3 and 6 μm as well as an onset of strong adsorption starting at about 8 μm consistent with the absorption of SiN passivation.

The input referred noise equivalent voltages of both NMOS and PMOS devices were also measured using the method discussed in [24] and shown in Fig. 13. The plots yield $K_f$ of 

![Graph](image)

Fig. 12. Responsivity vs. chopper frequency

![Graph](image)

Fig. 13. PMOS and NMOS input referred equivalent noise voltage

$6.6 \times 10^{-27}$ and $9.3 \times 10^{-26}$ A F, respectively. This permits the calculation of the expected detectivity.

The calculated detectivity $D*$ using Eqs. (19) and (14) with a detector area of $28 \times 42 \mu m^2$ is $D* = 8 \times 10^7 \text{ cm} \sqrt{\text{Hz W}^{-1}}$ at 30 Hz in reasonable agreement with our measurements. It is interesting to observe that the detectivity can be significantly increased if the area of the NMOS current source devices is enlarged because M4-M5 contribute about 4 times more noise power than suspended PMOS M1. This suggests that detectivities in the $10^8 \text{ cm} \sqrt{\text{Hz W}^{-1}}$ range are achievable.

H. Performance Comparison

Table I compares the detector parameters to those of other commercial available infrared detectors.

Compared to the most sensitive imaging-quality micro bolometer, the heat balancing detector has a higher responsivity but a higher noise originated from the active devices. However, the fabrication cost for the active pixel device is much lower due to its implementation within a conventional CMOS process. When compared to a non-imaging commercial pyroelectric detector, the heat balancing detector has much higher responsivity and about the same noise floor. In general, the heat balancing detector’s performance falls between the micro-bolometer and pyroelectric detector making it suitable for low cost, low-resolution imaging applications.

IV. AN 8 × 8 CMOS INFRARED IMAGER

A. A Single Pixel Design For 8 × 8 Infrared Imager

We implemented a simple 8 × 8 infrared imager using heat balancing detector pixels. The single pixel detector circuit used is shown in Fig. 14. The basic pixel configuration is very similar to the circuit shown in Fig.8. Each pixel consists of a bias control circuit, buffers, switches, and an external low pass filter. MOS Switches S1 and S2 are used to control the inputs to an external low pass filter that determines the bias voltage on the gate of M1 in standby mode. In the measure mode this voltage is stored in capacitor C1. The external low pass filter was implemented using a low noise chopper stabilized operational amplifier (LTC1053 from Linear Technology).

Fig.15 shows the imager organization. The chip consists of an 8 × 8 active pixel imager array, a 3 × 8 column decoder, a clock...
signal generator, one 8 x 1 analog multiplexer. The output signal of the chip is measured using an external locking amplifier controlled by a personal computer. Each row has a separate bias stabilization circuit which is shared by all the eight columns. Therefore, prior to reading each column, the bias voltage across capacitors C1 must be refreshed. Six different clocking signals which are exactly multiply of base clocking period (500 ms, 1 s, 2 s, 4 s, 8 s and 16 s) are generated using a pulse generator and multiplier. These signals drive the three signal inputs of column decoder and three row selection signals in analog multiplex. Therefore, a full scan of the whole imager takes 32 second to complete. The imager is fabricated using MOSIS 1.2 μm HP standard CMOS process followed by the post-processing pixel release. Several modifications were introduced to the pixel that improve the fabrication yield. Each individual pixel is suspended by two (rather than four) beams in a Y shape configuration. This layout reduces the etching time and improves the etching uniformity across the entire imager because it provides a larger opening for the etchant. The interconnection on the suspension beams was implemented using metal rather than polysilicon which does not require a good passivation coverage because it is not attacked by the TMAH solution. These modifications improve the fabrication yield at the expense of a lower fill factor (about 11%) and a lower thermal resistance. All the pixel N-wells are connected together to a common bias line dur-
ing the etch to insure equal biasing potentials. Fig. 16 shows the top view of two $8 \times 8$ imagers. The imager on the left is $1.7 \times 1.1$ mm$^2$ including the column decoder and sixty four single pixels. The imager on the right includes the biasing stabilization circuit in each pixel hence requiring a larger area.

B. Testing

In order to test the infrared imager we constructed a set up using an incandescent light source, collimated lens, silicon wafer and glass wafer with aluminum pattern to perform the primary testing. We used an incandescent lamp enclosed inside a box with a small opening as a point source. The point source is located 38 cm away from the collimated lens approximating a paraxial light source. A silicon wafer is used to filter out any optical signal with wavelength lower than 1.2 $\mu$m. An infrared camera system using the same set up is constructed as shown in Fig. 18. To properly focus the infrared signal, a convex germanium (Ge) lens ($f/1.0$) with 5 cm focal length is used. The distance between the infrared imager and the focusing lens is set up to form a $1.9 \times 1.9$mm$^2$ imager for any object radiating heats placed between the near point (68 cm) to infinity. A MIKRON M305 stable black body light source heated at 500 K is placed 1.2 meters away to calibrate the responsivity and NETD of this imager. The imager is mounted on one X-direction and one Y-direction microchopper which can precisely adjust the location of imager. A six inch aluminum optical chopper is mounted in front of the Ge lens. Fig. 19 shows a typical output waveform from the lock-in amplifier. The x-axis stands for the pixel number and y-axis is the RMS amplitude of the signal in the same frequency as the optical chopper. The switching transients are also recorded between pixel signals. Pixel number 1-8 have weaker signal than pixel number 43-48. Fig. 20 shows plots of the imager response to C and L shape test patterns.

V. SUMMARY

A sensitive heat balanced infrared detector was fabricated and tested. This device has a responsivity one order better than any available uncooled commercial detector but suffers from an increased noise floor due to the usage of MOS devices for temperature sensing. The detector is constructed using a regular CMOS process followed by an electrochemical n-well release technique. The measurements indicate a responsivity in the order of $10^6$ V/W can be accomplished. An $8 \times 8$ infrared imager using the same working principle was fabricated and tested. The CMOS imager shows potential for low cost camera systems.

VI. ACKNOWLEDGMENTS

We thank Dr. G. Zissis and Dr. L. Peterson of ERIM for providing valuable advice on the experimental setup. We also thank Professor K. D. Wise in University of Michigan, Dr. A. D. Oliver in Sandia National Laboratory for many valuable discussions and suggestions. This work was support by the Semiconductor Research Corporation under Contract MC-085-95.

REFERENCES


